Rogue Registers Referenced in the KM Driver

Revision: 14

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Public

Contents

ROGUE_CR_AXI_ACE_LITE_CONFIGURATION

Size 46

Address: 0x000038c0

Access: read-write

Member of groups: mars jones

47	46	45	44	43	42	41	40
-	ENABLE_FENCE_OUT (_)		OSID_SECURITY (_) ...				

39	38	37	36	35	34	33	32
OSID_SECURITY (_)			DISABLE_COHERENT_WRITELINEUNIQUE (_)	DISABLE_COHERENT_WRITE (_)	DISABLE_COHERENT_READ (_)	ARCACHE_CACHE_MAINTENANCE (_) ...	

31	30	29	28	27	26	25	24
ARCACHE_CACHE_MAINTENANCE (_)		ARCACHE_COHERENT (_)				AWCACHE_COHERENT (_) ...	

23	22	21	20	19	18	17	16
AWCACHE_COHERENT (_)		ARDOMAIN_BARRIER (_)		AWDOMAIN_BARRIER (_)		ARDOMAIN_CACHE_MAINTENANCE (_)	

15	14	13	12	11	10	9	8
AWDOMAIN_COHERENT (_)		ARDOMAIN_COHERENT (_)		ARDOMAIN_NON_SNOOPING (_)		AWDOMAIN_NON_SNOOPING (_)	

7	6	5	4	3	2	1	0
ARCACHE_NON_SNOOPING (_)				AWCACHE_NON_SNOOPING (_) ...			

AXI ACE-LITE configuration registers

Name	Type	MSB	LSB	Default
ENABLE_FENCE_OUT	_	45	45	0
OSID_SECURITY	_	44	37	0
DISABLE_COHERENT_WRITELINEUNIQUE	_	36	36	0
DISABLE_COHERENT_WRITE	_	35	35	0
DISABLE_COHERENT_READ	_	34	34	0
ARCACHE_CACHE_MAINTENANCE	_	33	30	0x2
ARCACHE_COHERENT	_	29	26	0x2

AWCACHE_COHERENT	_	25	22	0x2
ARDOMAIN_BARRIER	_	21	20	0
AWDOMAIN_BARRIER	_	19	18	0
ARDOMAIN_CACHE_MAINTENANCE	_	17	16	0
AWDOMAIN_COHERENT	_	15	14	0x1
ARDOMAIN_COHERENT	_	13	12	0x1
ARDOMAIN_NON_SNOOPING	_	11	10	0
AWDOMAIN_NON_SNOOPING	_	9	8	0
ARCACHE_NON_SNOOPING	_	7	4	0
AWCACHE_NON_SNOOPING	_	3	0	0

AWCACHE_NON_SNOOPING
Size 4

Write cache policy for non-snooping transactions

ARCACHE_NON_SNOOPING
Size 4

Read cache policy for non-snooping transactions

AWDOMAIN_NON_SNOOPING
Size 2

Write shareability domain for non-snooping transactions 00 = Non-Shareable 11 = System

ARDOMAIN_NON_SNOOPING
Size 2

Read shareability domain for non-snooping transactions 00 = Non-Shareable 11 = System

ARDOMAIN_COHERENT
Size 2

Read shareability domain for coherant transactions 01 = Inner Shareable 10 = Outer Shareable

AWDOMAIN_COHERENT
Size 2

Write shareability domain for coherant transactions 01 = Inner Shareable 10 = Outer Shareable

ARDOMAIN_CACHE_MAINTENANCE
Size 2

Read shareability domain for cache maintenance transactions 00 = Non-Shareable 01 = Inner Shareable 10 = Outer Shareable

AWDOMAIN_BARRIER
Size 2

Write shareability domain for barrier transactions 00 = Non-Shareable 01 = Inner Shareable 10 = Outer Shareable 11 = System

ARDOMAIN_BARRIER
Size 2

Read shareability domain for barrier transactions 00 = Non-Shareable 01 = Inner Shareable 10 = Outer Shareable 11 = System

AWCACHE_COHERENT
Size 4

Write cache policy for coherent transactions - bit[1] should be set to 1

ARCACHE_COHERENT
Size 4

Read cache policy for coherent transactions - bit[1] should be set to 1

ARCACHE_CACHE_MAINTENANCE
Size 4

Read cache policy for cache maintenance transactions - bit[1] should be set to 1

DISABLE_COHERENT_READ
Size 1

SET to 1 to disable coherent reads

DISABLE_COHERENT_WRITE
Size 1

SET to 1 to disable coherent writes

DISABLE_COHERENT_WRITELINEUNIQUE
Size 1

SET to 1 to disable coherent write line uniques

OSID_SECURITY
Size 8

SET to 1 to disable secure reads/writes for each OSID

ENABLE_FENCE_OUT
Size 1

SET to 1 to enable fence output to AXI

ROGUE_CR_BIF_CAT_BASE0
Size 40

Address: 0x00001200

Access: read-write

Member of groups: slc2 sidekick

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_)				*reserved*			

7	6	5	4	3	2	1	0
reserved							

Name	Type	MSB	LSB	Default
ADDR	_	39	12	0

ADDR
Size 28

ROGUE_CR_BIF_CAT_BASE1
Size 40

Address: 0x00001208

Access: read-write

Member of groups: slc2 sidekick

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_)				*reserved*			

7	6	5	4	3	2	1	0
reserved							

Name	Type	MSB	LSB	Default
ADDR	_	39	12	0

ADDR
Size 28

ROGUE_CR_BIF_FAULT_BANK0_MMU_STATUS
Size 16

Address: 0x000012b0

Access: readonly

Member of groups: tornado bifpmcache

15	14	13	12	11	10	9	8
CAT_BASE (_)				*reserved*	PAGE_SIZE (_)		

7	6	5	4	3	2	1	0

reserved	DATA_TYPE (_)	FAULT_RO (_)	*reserved*	FAULT_PM_META_RO (_)	*reserved*	FAULT (_) ...	

Indicates a fault has occurred on bank 0 and provides details of fault

Name	Type	MSB	LSB	Default
CAT_BASE	_	15	12	0
PAGE_SIZE	_	10	8	0
DATA_TYPE	_	6	5	0
FAULT_RO	_	4	4	0
FAULT_PM_META_RO	_	2	2	0
FAULT	_	0	0	0

CAT_BASE

Size 4

Catalogue base address number

PAGE_SIZE

Size 3

Page size

DATA_TYPE

Size 2

MMU data type that was invalid (on valid fault)

FAULT_RO

Size 1

Indicates read-only fault('1') or valid fault('0')

FAULT_PM_META_RO

Size 1

Indicates pm/meta protected region fault

FAULT

Size 1

Indicates a fault has occured

ROGUE_CR_BIF_FAULT_BANK0_REQ_STATUS

Size 53

Address: 0x000012b8

Access: readonly

Member of groups: tornado bifpmcache

55	54	53	52	51	50	49	48
-			RNW (_)	TAG_SB (_) ...			

47	46	45	44	43	42	41	40
TAG_SB (_)		TAG_ID (_)					

39	38	37	36	35	34	33	32
ADDRESS (_) ...							

31	30	29	28	27	26	25	24
ADDRESS (_) ...							

23	22	21	20	19	18	17	16
ADDRESS (_) ...							

15	14	13	12	11	10	9	8
ADDRESS (_) ...							

7	6	5	4	3	2	1	0
ADDRESS (_)				*reserved*			

Provides details of the request that faulted on bank 0

Name	Type	MSB	LSB	Default
RNW	_	52	52	0
TAG_SB	_	51	46	0
TAG_ID	_	45	40	0
ADDRESS	_	39	4	0

RNW
Size 1

TAG_SB
Size 6

TAG_ID
Size 6

ADDRESS
Size 36

ROGUE_CR_BIF_FAULT_BANK1_MMU_STATUS
Size 16

Address: 0x000012c0

Access: readonly

Member of groups: sidekick2 sidekick

15	14	13	12	11	10	9	8
CAT_BASE (_)				*reserved*	PAGE_SIZE (_)		

7	6	5	4	3	2	1	0
reserved	DATA_TYPE (_)	FAULT_RO (_)		*reserved*	FAULT_PM_META_RO (_)	*reserved*	FAULT (_) ...

Indicates a fault has occurred on bank 1 and provides details of fault

Name	MSB	LSB	Default
CAT_BASE	15	12	0
PAGE_SIZE	10	8	0

DATA_TYPE	6	5	0
FAULT_RO	4	4	0
FAULT_PM_META_RO	2	2	0
FAULT	0	0	0

CAT_BASE
Size 4

Catalogue base address number

PAGE_SIZE
Size 3

Page size

DATA_TYPE
Size 2

MMU data type that was invalid (on valid fault)

FAULT_RO
Size 1

Indicates read-only fault('1') of valid fault('0')

FAULT_PM_META_RO
Size 1

Indicates pm/meta protected region fault

FAULT
Size 1

Indicates a fault has occured

ROGUE_CR_BIF_FAULT_BANK1_REQ_STATUS
Size 51

Address: 0x000012c8

Access: readonly

Member of groups: sidekick2 sidekick

55	54	53	52	51	50	49	48
-					RNW (_)	TAG_SB (_) ...	

47	46	45	44	43	42	41	40
TAG_SB (_)				TAG_ID (_)			

39	38	37	36	35	34	33	32
ADDRESS (_) ...							

31	30	29	28	27	26	25	24
ADDRESS (_) ...							

23	22	21	20	19	18	17	16

ADDRESS (_) ...

15	14	13	12	11	10	9	8
ADDRESS (_) ...							

7	6	5	4	3	2	1	0
ADDRESS (_)				*reserved*			

Provides details of the request that faulted on bank 1

Name	MSB	LSB	Default
RNW	50	50	0
TAG_SB	49	44	0
TAG_ID	43	40	0
ADDRESS	39	4	0

RNW
Size 1

TAG_SB
Size 6

TAG_ID
Size 4

ADDRESS
Size 36

ROGUE_CR_BIF_MMU_ENTRY
Size 2

Address: 0x00001290

Access: read-write

Member of groups: slc2 sidekick

7	6	5	4	3	2	1	0
-						ENABLE (_)	PENDING (_) ...

Indicates MMU is waiting on the driver to map an entry

Name	MSB	LSB	Default
ENABLE	1	1	0
PENDING	0	0	0

ENABLE
Size 1

When set, PENDING will trigger an interrupt back to the host CPU (bypassing the FW)

PENDING
Size 1

ROGUE_CR_BIF_MMU_ENTRY_STATUS

Size 40

Address: 0x00001288

Access: readonly

Member of groups: slc2 sidekick

39	38	37	36	35	34	33	32
ADDRESS (_) ...							

31	30	29	28	27	26	25	24
ADDRESS (_)							

23	22	21	20	19	18	17	16
ADDRESS (_) ...							

15	14	13	12	11	10	9	8
ADDRESS (_)				*reserved*			

7	6	5	4	3	2	1	0
CAT_BASE (_)				*reserved*		DATA_TYPE (_) ...	

Status of pending entry

Name	MSB	LSB	Default
ADDRESS	39	12	0
CAT_BASE	7	4	0
DATA_TYPE	1	0	0

ADDRESS

Size 28

Virtual 4KB address

CAT_BASE

Size 4

Catalogue base address number

DATA_TYPE

Size 2

MMU data type "00" = PT, "01" = PD, "10" = PC

ROGUE_CR_BIFPM_READS_EXT_STATUS

Size 16

Address: 0x00001338

Access: readonly

Member of groups: tornado bifpmcache

15	14	13	12	11	10	9	8
BANK0 (_) ...							

7	6	5	4	3	2	1	0

BANK0 (_) ...

Outstanding 256-bit read data external to BIF for BIF256

Name	Type	MSB	LSB	Default
BANK0	_	15	0	0

BANK0
Size 16

ROGUE_CR_BIFPM_STATUS_MMU
Size 8

Address: 0x00001350

Access: readonly

Member of groups: tornado bifpmcache

7	6	5	4	3	2	1	0
REQUESTS (_) ...							

Outstanding MMU requests from BIF0

Name	Type	MSB	LSB	Default
REQUESTS	_	7	0	0

REQUESTS
Size 8

ROGUE_CR_BIF_READS_EXT_STATUS
Size 28

Address: 0x00001320

Access: readonly

Member of groups: slc2 sidekick2 sidekick

31	30	29	28	27	26	25	24
-				MMU (_) ...			

23	22	21	20	19	18	17	16
MMU (_)							

15	14	13	12	11	10	9	8
BANK1 (_) ...							

7	6	5	4	3	2	1	0
BANK1 (_) ...							

Outstanding read data external to BIF for BIF128 and MMU

Name	Type	MSB	LSB	Default
MMU	_	27	16	0
BANK1	_	15	0	0

MMU
Size 12

BANK1
Size 16

ROGUE_CR_BIF_STATUS_MMU
Size 8

Address: 0x00001358

Access: readonly

Member of groups: sidekick2 sidekick

7	6	5	4	3	2	1	0
REQUESTS (_) ...							

Outstanding MMU requests from BIF1

Name	Type	MSB	LSB	Default
REQUESTS	_	7	0	0

REQUESTS
Size 8

ROGUE_CR_BIF_TRUST
Size 21

Address: 0x0000a000

Access: read-write

Member of groups: BI texas bifpmcache mars

23	22	21	20	19	18	17	16
-			*reserved*				ENABLE (_)

15	14	13	12	11	10	9	8
DM_TRUSTED (DM)							OTHER_COMPUTE_DM_TRUSTED (_)

7	6	5	4	3	2	1	0
MCU_COMPUTE_DM_TRUSTED (_)	PBE_COMPUTE_DM_TRUSTED (_)	OTHER_PIXEL_DM_TRUSTED (_)	MCU_PIXEL_DM_TRUSTED (_)	PBE_PIXEL_DM_TRUSTED (_)	OTHER_VERTEX_DM_TRUSTED (_)	MCU_VERTEX_DM_TRUSTED (_)	PBE_VERTEX_DM_TRUSTED (_) ...

Define Requestors/Data Masters which are Trusted/Untrusted and enable/disable the Memory Bus Security feature within the Core When enabled the GPU will emit the security signals out through the external memory interface.

Name	Type	MSB	LSB	Default
ENABLE	_	16	16	0
DM_TRUSTED	DM	15	9	0
OTHER_COMPUTE_DM_TRUSTED	_	8	8	0
MCU_COMPUTE_DM_TRUSTED	_	7	7	0
PBE_COMPUTE_DM_TRUSTED	_	6	6	0
OTHER_PIXEL_DM_TRUSTED	_	5	5	0
MCU_PIXEL_DM_TRUSTED	_	4	4	0
PBE_PIXEL_DM_TRUSTED	_	3	3	0
OTHER_VERTEX_DM_TRUSTED	_	2	2	0
MCU_VERTEX_DM_TRUSTED	_	1	1	0
PBE_VERTEX_DM_TRUSTED	_	0	0	0

DM
Size 7

TYPE
Size 7

7	6	5	4	3	2	1	0
-	PM_ALIST (_)	HOST (_)	META (_)	PB_ZLS (_)	PB_TE (_)	PB_VCE (_)	*reserved*

Name	Type	MSB	LSB	Default
PM_ALIST	_	6	6	---
HOST	_	5	5	---
META	_	4	4	---
PB_ZLS	_	3	3	---
PB_TE	_	2	2	---
PB_VCE	_	1	1	---

PB_VCE
Size 1

PB_TE
Size 1

PB_ZLS
Size 1

META
Size 1

HOST
Size 1

PM_ALIST
Size 1

PBE_VERTEX_DM_TRUSTED
Size 1

Defines whether PBE accesses with the Vertex DM are trusted: 0x1 = Trusted, 0x0 = Untrusted

MCU_VERTEX_DM_TRUSTED
Size 1

Defines whether MCU accesses with the Vertex DM are trusted: 0x1 = Trusted, 0x0 = Untrusted

OTHER_VERTEX_DM_TRUSTED
Size 1

Defines whether other accesses with the Vertex DM are trusted: 0x1 = Trusted, 0x0 = Untrusted

PBE_PIXEL_DM_TRUSTED
Size 1

Defines whether PBE accesses with the Pixel DM are trusted: 0x1 = Trusted, 0x0 = Untrusted

MCU_PIXEL_DM_TRUSTED
Size 1

Defines whether MCU accesses with the Pixel DM are trusted: 0x1 = Trusted, 0x0 = Untrusted

OTHER_PIXEL_DM_TRUSTED
Size 1

Defines whether other accesses with the Pixel DM are trusted: 0x1 = Trusted, 0x0 = Untrusted

PBE_COMPUTE_DM_TRUSTED
Size 1

Defines whether PBE accesses with the Compute DM are trusted: 0x1 = Trusted, 0x0 = Untrusted

MCU_COMPUTE_DM_TRUSTED
Size 1

Defines whether MCU accesses with the Compute DM are trusted: 0x1 = Trusted, 0x0 = Untrusted

OTHER_COMPUTE_DM_TRUSTED
Size 1

Defines whether other accesses with the Compute DM are trusted: 0x1 = Trusted, 0x0 = Untrusted

ENABLE
Size 1

Enable Security feature: 0x1 = Enabled, 0x0 = Disabled

ROGUE_CR_BLACKPEARL_PERF
Size 7

Address: 0x00008400

Access: read-write

Member of groups: blackpearl_perf

7	6	5	4	3	2	1	0
-	CLR_5 (_)	CLR_4 (_)	CLR_3 (_)	CLR_2 (_)	CLR_1 (_)	CLR_0 (_)	CTRL_ENABLE (_) ...

Name	MSB	LSB	Default
CLR_5	6	6	0
CLR_4	5	5	0
CLR_3	4	4	0
CLR_2	3	3	0
CLR_1	2	2	0
CLR_0	1	1	0
CTRL_ENABLE	0	0	0

CLR_5
Size 1

clear counter 3

CLR_4
Size 1

clear counter 3

CLR_3
Size 1

clear counter 3

CLR_2
Size 1

clear counter 2

CLR_1
Size 1

clear counter 1

ROGUE_CR_BLACKPEARL_PERF_COUNTER_0
Size 32

Address: 0x00008448

Access: readonly

Member of groups: blackpearl_perf

31	30	29	28	27	26	25	24
REG (_) ...							

23	22	21	20	19	18	17	16
REG (_) ...							

15	14	13	12	11	10	9	8
REG (_) ...							

7	6	5	4	3	2	1	0
REG (_) ...							

Name	MSB	LSB	Default
REG	31	0	0

REG
Size 32

counter a0

ROGUE_CR_blackpearl_perf_INDIRECT
Size 2

Address: 0x000083f8

Access: read-write

Member of groups: blackpearl_perf

7	6	5	4	3	2	1	0
-						ADDRESS (_) ...	

Name	MSB	LSB	Default
ADDRESS	1	0	---

ROGUE_CR_BLACKPEARL_PERF_SELECT0

Size 64

Address: 0x00008408

Access: read-write

Member of groups: blackpearl_perf

63	62	61	60	59	58	57	56
reserved						BATCH_MAX (_) ...	

55	54	53	52	51	50	49	48
BATCH_MAX (_)							

47	46	45	44	43	42	41	40
reserved						BATCH_MIN (_) ...	

39	38	37	36	35	34	33	32
BATCH_MIN (_)							

31	30	29	28	27	26	25	24
MODE (_)	*reserved*						

23	22	21	20	19	18	17	16
reserved						GROUP_SELECT (_)	

15	14	13	12	11	10	9	8
BIT_SELECT (_) ...							

7	6	5	4	3	2	1	0
BIT_SELECT (_) ...							

Name	MSB	LSB	Default
BATCH_MAX	61	48	0x3fff
BATCH_MIN	45	32	0
MODE	31	31	0
GROUP_SELECT	21	16	0
BIT_SELECT	15	0	0

BATCH_MAX

Size 14

this is the max batch number which will be counted in this group

BATCH_MIN
Size 14

this is the min batch number which will be counted in this group

MODE
Size 1

reduction mode, 0: bitwise increments, 1: unsigned count increment

GROUP_SELECT
Size 6

group select, see full PERF documentation for signals in each group

BIT_SELECT
Size 16

bit mask for enabled signals in group

ROGUE_CR_CLK_CTRL
Size 64

Address: 0x00000000

Access: read-write

Member of groups: rascal blackpearl jones pbe texas3 texas tornado slc3 slc2 slc tpu tpu_mcu_l0 usc bifpmcache ta rasterisation hub sidekick2 sidekick

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved		USCS (MODE) = *AUTO*		PBE (MODE) = *AUTO*		MCU_l1 (MODE) = *AUTO*	

47	46	45	44	43	42	41	40
CDM (MODE) = *AUTO*		SIDEKICK (MODE) = *AUTO*		BIF_SIDEKICK (MODE) = *AUTO*		BIF (MODE) = *AUTO*	

39	38	37	36	35	34	33	32
reserved							

31	30	29	28	27	26	25	24
reserved		TPU_MCU_DEMUX (MODE) = *AUTO*		MCU_L0 (MODE) = *AUTO*		TPU (MODE) = *AUTO*	

23	22	21	20	19	18	17	16
reserved		USC (MODE) = *AUTO*		*reserved*		SLC (MODE) = *AUTO*	

15	14	13	12	11	10	9	8
UVS (MODE) = *AUTO*		PDS (MODE) = *AUTO*		VDM (MODE) = *AUTO*		PM (MODE) = *AUTO*	

7	6	5	4	3	2	1	0
GPP (MODE) = *AUTO*		TE (MODE) = *AUTO*		TSP (MODE) = *AUTO*		ISP (MODE) ... = *AUTO*	

Core Module Clock Control Modes. Allows individual domain clocks to be forced off, forced on or operate under automatic pipeline activity based clock gating. This register is generally controlled by the GPU firmware and should be set to AUTO. Clock gating reduces the power consumed by the device.

Name	Type	MSB	LSB	Default

USCS	MODE	53	52	AUTO [0x2]
PBE	MODE	51	50	AUTO [0x2]
MCU_l1	MODE	49	48	AUTO [0x2]
CDM	MODE	47	46	AUTO [0x2]
SIDEKICK	MODE	45	44	AUTO [0x2]
BIF_SIDEKICK	MODE	43	42	AUTO [0x2]
BIF	MODE	41	40	AUTO [0x2]
TPU_MCU_DEMUX	MODE	29	28	AUTO [0x2]
MCU_L0	MODE	27	26	AUTO [0x2]
TPU	MODE	25	24	AUTO [0x2]
USC	MODE	21	20	AUTO [0x2]
SLC	MODE	17	16	AUTO [0x2]
UVS	MODE	15	14	AUTO [0x2]
PDS	MODE	13	12	AUTO [0x2]
VDM	MODE	11	10	AUTO [0x2]
PM	MODE	9	8	AUTO [0x2]
GPP	MODE	7	6	AUTO [0x2]
TE	MODE	5	4	AUTO [0x2]
TSP	MODE	3	2	AUTO [0x2]
ISP	MODE	1	0	AUTO [0x2]

MODE

Size 2

Possible Values:

Name	Value/Range	Info
OFF	0 [0]	The domain clock is forced off
ON	1 [0x1]	The domain clock is forced on
AUTO	2 [0x2]	Automatic clock gating is active, the domain clock is only on whilst data is being processed

ROGUE_CR_CLK_CTRL2

Size: 64

Address: 0x00000090**Default:** 0x0000000002aaaaaa

Type: Register**Direction**: read-write**SCOPE:** SYSTEM

Register banks: rac_dv rac jones tpu_dv tpu usc

Kick pipeline: global

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32

reserved

31	30	29	28	27	26	25	24
reserved						RTS (MODE) = *AUTO*	

23	22	21	20	19	18	17	16
PCG (MODE) = *AUTO*		BPS (MODE) = *AUTO*		RS (MODE) = *AUTO*		RRC (MODE) = *AUTO*	

15	14	13	12	11	10	9	8
URI (MODE) = *AUTO*		RCE (MODE) = *AUTO*		ASC (MODE) = *AUTO*		FP (MODE) = *AUTO*	

7	6	5	4	3	2	1	0
INT (MODE) = *AUTO*		YUV (MODE) = *AUTO*		USC_PIPE_PAP_DOT8 (MODE) = *AUTO*		USC_PIPE_PAP_FOP (MODE) ... = *AUTO*	

Core Module Clock Control Modes. Allows individual domain clocks to be forced off, forced on or operate under automatic pipeline activity based clock gating. This register is generally controlled by the GPU firmware and should be set to AUTO. Clock gating reduces the power consumed by the device.

Name	MSB	LSB	Default	Description	Bank Filter
RTS	25	24	AUTO [0x2]		rac rac_dv
PCG	23	22	AUTO [0x2]		rac rac_dv
BPS	21	20	AUTO [0x2]		rac rac_dv
RS	19	18	AUTO [0x2]		rac rac_dv
RRC	17	16	AUTO [0x2]		rac rac_dv
URI	15	14	AUTO [0x2]		rac rac_dv
RCE	13	12	AUTO [0x2]		jones rac_dv
ASC	11	10	AUTO [0x2]		jones rac_dv
FP	9	8	AUTO [0x2]		tpu tpu_dv rac_dv
INT	7	6	AUTO [0x2]		tpu tpu_dv rac_dv
YUV	5	4	AUTO [0x2]		tpu tpu_dv rac_dv
USC_PIPE_PAP_DOT8	3	2	AUTO [0x2]		usc rac_dv
USC_PIPE_PAP_FOP	1	0	AUTO [0x2]		usc rac_dv

ROGUE_CR_CLK_CTRL2.MODE

Size: 2

Type: Define**Possible Values:**

Name	Value/Range	Info
OFF	0 [0]	The domain clock is forced off
ON	1 [0x1]	The domain clock is forced on
AUTO	2 [0x2]	Automatic clock gating is active, the domain clock is only on whilst data is being processed

ROGUE_CR_CORE_ID

Size 64

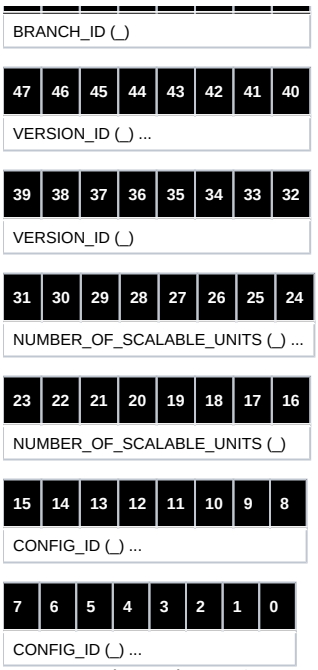
Address: 0x00000020

Access: readonly

Member of groups: jones mars

63	62	61	60	59	58	57	56
BRANCH_ID (_) ...							

55	54	53	52	51	50	49	48



Reports the product ID Core ID Register

Name	Type	MSB	LSB	Default
BRANCH_ID	_	63	48	---
VERSION_ID	_	47	32	---
NUMBER_OF_SCALABLE_UNITS	_	31	16	---
CONFIG_ID	_	15	0	---

BRANCH_ID

Size 16

B - Branch ID

VERSION_ID

Size 16

V - Version ID

NUMBER_OF_SCALABLE_UNITS

Size 16

N - Number of scalable Units

CONFIG_ID

Size 16

C - Config ID

ROGUE_CR_CORE_REVISION

Size 32

Address: 0x00000020

Access: readonly

Member of groups: jones sidekick2 sidekick

31	30	29	28	27	26	25	24
DESIGNER (_)							

23	22	21	20	19	18	17	16
MAJOR (_)							

15	14	13	12	11	10	9	8
MINOR (_)							

7	6	5	4	3	2	1	0
MAINTENANCE (_) ...							

Reports the core revision Core Revision Register identifies the specific core revision. This is updated to reflect the formal release status of the core.

Name	MSB	LSB	Default
DESIGNER	31	24	0
MAJOR	23	16	0x1
MINOR	15	8	0
MAINTENANCE	7	0	0

DESIGNER
Size 8

Designer Field

MAJOR
Size 8

Major Revision

MINOR
Size 8

Minor Revision

MAINTENANCE
Size 8

Maintenance Revision

ROGUE_CR_ECC_RAM_INIT_DONE
Size 5

Address: 0x0000f350

Access: readonly

Member of groups: rascal slc tpu_mcu_l0 usc sidekick mars

7	6	5	4	3	2	1	0
-			SLC_SIDEKICK (_)	USC (_)	TPU_MCU_L0 (_)	RASCAL (_)	*reserved*

Core ECC RAM initialisation status register. Read this register to determine the initialisation status of ECC RAMs on all RAMs in the corresponding block

Name	Type	MSB	LSB	Default
SLC_SIDEKICK	_	4	4	0
USC	_	3	3	0

TPU_MCU_L0	_	2	2	0
RASCAL	_	1	1	0

RASCAL
Size 1

ECC_RAM Init kick for ALL blocks within RASCAL

TPU_MCU_L0
Size 1

ECC_RAM Init kick for ALL blocks within TPU_MCU_L0

USC
Size 1

ECC_RAM Init kick for ALL blocks within USC

SLC_SIDEKICK
Size 1

ECC_RAM Init kick for ALL blocks within SLC_SIDEKICK

ROGUE_CR_ECC_RAM_INIT_KICK
Size 5

Address: 0x0000f348

Access: writeonly

Member of groups: rascal slc tpu_mcu_l0 usc sidekick mars

7	6	5	4	3	2	1	0
-			SLC_SIDEKICK (_)	USC (_)	TPU_MCU_L0 (_)	RASCAL (_)	*reserved*

Core ECC RAM Initialisation control register. Write a '1' to initate ECC RAM self initialisation for all RAMs in the corresponding block and a '0' to clear

Name	Type	MSB	LSB	Default
SLC_SIDEKICK	_	4	4	0
USC	_	3	3	0
TPU_MCU_L0	_	2	2	0
RASCAL	_	1	1	0

RASCAL
Size 1

ECC_RAM Init kick for ALL blocks within RASCAL

TPU_MCU_L0
Size 1

ECC_RAM Init kick for ALL blocks within TPU_MCU_L0

USC
Size 1

ECC_RAM Init kick for ALL blocks within USC

SLC_SIDEKICK

Size 1

ECC_RAM Init kick for ALL blocks within SLC_SIDEKICK

ROGUE_CR_EVENT_STATUS

Size 32

Address: 0x00000130

Access: read-write

Member of groups: mars

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved			SAFETY (_)	SLAVE_REQ (_)	*reserved*		

15	14	13	12	11	10	9	8
USC_TRIGGER (_)	ZLS_FINISHED (_)	GPIO_ACK (_)	GPIO_REQ (_)	POWER_ABORT (_)	POWER_COMPLETE (_)	MMU_PAGE_FAULT (_)	PM_3D_MEM_FREE (_)

7	6	5	4	3	2	1	0
PM_OUT_OF_MEMORY (_)	TA_TERMINATE (_)	TA_FINISHED (_)	ISP_END_MACROTILE (_)	PIXELBE_END_RENDER (_)	COMPUTE_FINISHED (_)	KERNEL_FINISHED (_)	*reserved*

The event status register indicate the source of an interrupt generated by PowerVR RGX These events only schedule an interrupt context thread to run on META when the appropriate enables are set in ROGUE_CR_DMn_INTERRUPT_ENABLE

Name	Type	MSB	LSB	Default
SAFETY	_	20	20	---
SLAVE_REQ	_	19	19	---
USC_TRIGGER	_	15	15	---
ZLS_FINISHED	_	14	14	---
GPIO_ACK	_	13	13	---
GPIO_REQ	_	12	12	---
POWER_ABORT	_	11	11	---
POWER_COMPLETE	_	10	10	---
MMU_PAGE_FAULT	_	9	9	---
PM_3D_MEM_FREE	_	8	8	---
PM_OUT_OF_MEMORY	_	7	7	---
TA_TERMINATE	_	6	6	---
TA_FINISHED	_	5	5	---
ISP_END_MACROTILE	_	4	4	---
PIXELBE_END_RENDER	_	3	3	---
COMPUTE_FINISHED	_	2	2	---
KERNEL_FINISHED	_	1	1	---

SAFETY

Size 1

Indicates an interrupt event from an active safety feature has been received

SLAVE_REQ
Size 1

Indicates an interrupt event from a slave has been received.

USC_TRIGGER
Size 1

One or more USC has executed a nop.trigger instruction

ZLS_FINISHED
Size 1

ZLS has finished all tiles in a Render

GPIO_ACK
Size 1

General Purpose ouput acknowledgement

GPIO_REQ
Size 1

General Purpose input request

POWER_ABORT
Size 1

The requested power operation has been denied.

POWER_COMPLETE
Size 1

The requested power operation has completed

MMU_PAGE_FAULT
Size 1

An MMU page fault has occurred

PM_3D_MEM_FREE
Size 1

PM memory allocation completed for the current render

PM_OUT_OF_MEMORY
Size 1

PM memory allocation failed for a macro-tile

TA_TERMINATE
Size 1

The TE has aborted a macro tile after a failted PM allocation request

TA_FINISHED
Size 1

The TA phase has completed

ISP_END_MACROTILE
Size 1

ISP End-of-Macrotile

PIXELBE_END_RENDER
Size 1

The 3D phase has completed

COMPUTE_FINISHED
Size 1

The compute phase has completed

KERNEL_FINISHED
Size 1

A compute kernel has completed and updated the associated event object in external memory

---

ROGUE_CR_FWCORE_ADDR_REMAP_CONFIG0
Size 63

Address: 0x00003000

Access: read-write

Member of groups: mars

63	62	61	60	59	58	57	56
-	TRUSTED (_)	LOAD_STORE_EN (_)	FETCH_EN (_)	SIZE (_) ...			

55	54	53	52	51	50	49	48
SIZE (_) ...							

47	46	45	44	43	42	41	40
SIZE (_)				*reserved*	CBASE (_)		

39	38	37	36	35	34	33	32
DEVVADDR (_) ...							

31	30	29	28	27	26	25	24
DEVVADDR (_) ...							

23	22	21	20	19	18	17	16
DEVVADDR (_) ...							

15	14	13	12	11	10	9	8
DEVVADDR (_)				*reserved*			

7	6	5	4	3	2	1	0
reserved							

Override swerv memory access for this region

Name	Type	MSB	LSB	Default
TRUSTED	_	62	62	0
LOAD_STORE_EN	_	61	61	0
FETCH_EN	_	60	60	0
SIZE	_	59	44	0
CBASE	_	42	40	0
DEVVADDR	_	39	12	0xe1c0000

TRUSTED
Size 1

Set whether accesses in the this region are trusted

LOAD_STORE_EN
Size 1

Region enabled for loads/stores

FETCH_EN
Size 1

Region enabled for instruction fetches

SIZE
Size 16

Region mapped window size

CBASE
Size 3

MMU catalogue base index. Indices 0-7 are supported

DEVVADDR
Size 28

Base output address (4k aligned)

ROGUE_CR_FWCORE_BOOT
Size 1

Address: 0x00003090

Access: read-write

Member of groups: mars

7	6	5	4	3	2	1	0
-							ENABLE (_) ...

Boot the RISCV CPU

Name	Type	MSB	LSB	Default
ENABLE	_	0	0	0

ENABLE
Size 1

Boot the RISCV CPU

ROGUE_CR_FWCORE_MEM_CAT_BASE0
Size 40

Address: 0x000030f0

Access: read-write

Member of groups: mars

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_)				*reserved*			

7	6	5	4	3	2	1	0
reserved							

Name	Type	MSB	LSB	Default
ADDR	_	39	12	0

ADDR
Size 28

ROGUE_CR_FWCORE_MEM_CAT_BASE1
Size 40

Address: 0x000030f8

Access: read-write

Member of groups: mars

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_)				*reserved*			

7	6	5	4	3	2	1	0

reserved

Name	Type	MSB	LSB	Default
ADDR	_	39	12	0

ADDR
Size 28

ROGUE_CR_GARTEN_SLC
Size 1

Address: 0x00000bb8

Access: read-write

Member of groups: jones

7	6	5	4	3	2	1	0
-							FORCE_COHERENCY (_) ...

Override Garten SLC accesses to be Coherent with memory when register written with 1 (default value is SLC coherency enabled)

Name	MSB	LSB	Default
FORCE_COHERENCY	0	0	0x1

FORCE_COHERENCY
Size 1

0 = SLC control, 1 = SLC Coherency Forced

ROGUE_CR_HUB_BIFPMCACHE_PERF
Size 5

Address: 0x00007800

Access: read-write

Member of groups: hub_bifpmcache_perf

7	6	5	4	3	2	1	0
-			CLR_3 (_)	CLR_2 (_)	CLR_1 (_)	CLR_0 (_)	CTRL_ENABLE (_) ...

Name	Type	MSB	LSB	Default
CLR_3	_	4	4	0
CLR_2	_	3	3	0
CLR_1	_	2	2	0
CLR_0	_	1	1	0
CTRL_ENABLE	_	0	0	0

CLR_3
Size 1

clear counter 3

CLR_2
Size 1

clear counter 2

CLR_1
Size 1

clear counter 1

CLR_0
Size 1

clear counter 0

CTRL_ENABLE
Size 1

enables the perf bus counters

ROGUE_CR_HUB_BIFPMCACHE_PERF_COUNTER_0
Size 32

Address: 0x00007850

Access: readonly

Member of groups: hub_bifpmcache_perf

31	30	29	28	27	26	25	24
REG (_) ...							

23	22	21	20	19	18	17	16
REG (_) ...							

15	14	13	12	11	10	9	8
REG (_) ...							

7	6	5	4	3	2	1	0
REG (_) ...							

Name	Type	MSB	LSB	Default
REG	_	31	0	0

REG
Size 32

counter a0

ROGUE_CR_HUB_BIFPMCACHE_PERF_SELECT0
Size 64

Address: 0x00007808

Access: read-write

Member of groups: hub_bifpmcache_perf

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
reserved							

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved		MODE (_)	GROUP_SELECT (_)				

15	14	13	12	11	10	9	8
BIT_SELECT (_) ...							

7	6	5	4	3	2	1	0
BIT_SELECT (_) ...							

Name	Type	MSB	LSB	Default
MODE	_	21	21	0
GROUP_SELECT	_	20	16	0
BIT_SELECT	_	15	0	0

MODE
Size 1

reduction mode, 0: bitwise increments, 1: unsigned count increment

GROUP_SELECT
Size 5

group select, see full PERF hub_bifpmcache documentation for signals in each group

BIT_SELECT
Size 16

bit mask for enabled signals in group

ROGUE_CR_IRQ_OS0_EVENT_CLEAR
Size 32

Address: 0x00000be8

Access: read-write

Member of groups: mars

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved							

15	14	13	12	11	10	9	8
reserved							

7	6	5	4	3	2	1	0
reserved							SOURCE (_) ...

This register clears a per-OS host interrupt.

Name	Type	MSB	LSB	Default
SOURCE	_	0	0	0

SOURCE

Size 1

ROGUE_CR_IRQ_OS0_EVENT_STATUS

Size 32

Address: 0x00000bd8

Access: readonly

Member of groups: mars

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved							

15	14	13	12	11	10	9	8
reserved							

7	6	5	4	3	2	1	0
reserved							SOURCE (_) ...

This register indicates the source of a per-OS host interrupt. This register is set by the firmware and cleared by the host.

Name	Type	MSB	LSB	Default
SOURCE	_	0	0	0

SOURCE

Size 1

ROGUE_CR_JONES_IDLE

Size: 19

Address: 0x00008328**Default:** N/A

Type: Register**Direction**: read-only**GENERATE_POL:** NO

Register banks: jones

Kick pipeline: global

23	22	21	20	19	18	17	16
-					ASC (_)	RCE (_)	AXI2IMG (_)

15	14	13	12	11	10	9	8
SLC (_)	TDM (_)	FB_CDC_TLA (_)	FB_CDC (_)	MMU (_)	DFU (_)	GARTEN (_)	*reserved*

7	6	5	4	3	2	1	0
SOCIF (_)	TILING (_)	IPP (_)	USC_GMUTEX (_)	PM (_)	CDM (_)	DCE (_)	BIF (_) ...

Name	MSB	LSB	Default	Description	Bank Filter
ASC	18	18	0x1	ASC Module IDLE	jones
RCE	17	17	0x1	RCE Module IDLE	jones
AXI2IMG	16	16	0x1	AXI2IMG Module IDLE	jones
SLC	15	15	0x1	SLC Module IDLE	jones
TDM	14	14	0x1	TDM Module IDLE	jones
FB_CDC_TLA	13	13	0x1	FB CDC Module IDLE	jones
FB_CDC	12	12	0x1	FB CDC Module IDLE	jones
MMU	11	11	0x1	MMU Module IDLE	jones
DFU	10	10	0x1	Jones DFU Module IDLE	jones
GARTEN	9	9	0x1	GARTEN Module IDLE	jones
SOCIF	7	7	0x1	SOCIF Module IDLE	jones
TILING	6	6	0x1	TILING Module IDLE	jones
IPP	5	5	0x1	IPP Module IDLE	jones
USC_GMUTEX	4	4	0x1	USC Global Mutex Module IDLE	jones
PM	3	3	0x1	PM Module IDLE	jones
CDM	2	2	0x1	CDM Module IDLE	jones
DCE	1	1	0x1	DCE Module IDLE	jones
BIF	0	0	0x1	JONES BIF Module IDLE	jones

ROGUE_CR_JONES_IDLE.ASC

Size: 1

Type: Define

ASC Module IDLE

ROGUE_CR_JONES_IDLE.RCE

Size: 1

Type: Define

RCE Module IDLE

ROGUE_CR_JONES_IDLE.AXI2IMG

Size: 1

Type: Define

AXI2IMG Module IDLE

ROGUE_CR_JONES_IDLE.SLC

Size: 1

Type: Define

SLC Module IDLE

ROGUE_CR_JONES_IDLE.TDM

Size: 1

Type: Define

TDM Module IDLE

ROGUE_CR_JONES_IDLE.FB_CDC_TLA

Size: 1

Type: Define

FB CDC Module IDLE

ROGUE_CR_JONES_IDLE.FB_CDC

Size: 1

Type: Define

FB CDC Module IDLE

ROGUE_CR_JONES_IDLE.MMU

Size: 1

Type: Define

MMU Module IDLE

ROGUE_CR_JONES_IDLE.DFU

Size: 1

Type: Define

Jones DFU Module IDLE

ROGUE_CR_JONES_IDLE.GARTEN

Size: 1

Type: Define

GARTEN Module IDLE

ROGUE_CR_JONES_IDLE.SOCIF

Size: 1

Type: Define

SOCIF Module IDLE

ROGUE_CR_JONES_IDLE.TILING

Size: 1

Type: Define

TILING Module IDLE

ROGUE_CR_JONES_IDLE.IPP

Size: 1

Type: Define

IPP Module IDLE

ROGUE_CR_JONES_IDLE.USC_GMUTEX

Size: 1

Type: Define

USC Global Mutex Module IDLE

ROGUE_CR_JONES_IDLE.PM

Size: 1

Type: Define

PM Module IDLE

ROGUE_CR_JONES_IDLE.CDM

Size: 1

Type: Define

CDM Module IDLE

ROGUE_CR_JONES_IDLE.DCE

Size: 1

Type: Define

DCE Module IDLE

ROGUE_CR_JONES_IDLE.BIF

Size: 1

Type: Define

JONES BIF Module IDLE

ROGUE_CR_JONES_PERF

Size 5

Address: 0x00008330

Access: read-write

Member of groups: jones_perf

7	6	5	4	3	2	1	0
-			CLR_3 (_)	CLR_2 (_)	CLR_1 (_)	CLR_0 (_)	CTRL_ENABLE (_) ...

Name	MSB	LSB	Default
CLR_3	4	4	0
CLR_2	3	3	0
CLR_1	2	2	0
CLR_0	1	1	0
CTRL_ENABLE	0	0	0

CLR_3

Size 1

clear counter 3

CLR_2

Size 1

clear counter 2

CLR_1
Size 1

clear counter 1

CLR_0
Size 1

clear counter 0

CTRL_ENABLE
Size 1

enables the perf bus counters

ROGUE_CR_JONES_PERF_COUNTER_0
Size 32

Address: 0x00008368

Access: readonly

Member of groups: jones_perf

31	30	29	28	27	26	25	24
REG (_) ...							

23	22	21	20	19	18	17	16
REG (_) ...							

15	14	13	12	11	10	9	8
REG (_) ...							

7	6	5	4	3	2	1	0
REG (_) ...							

Name	MSB	LSB	Default
REG	31	0	0

REG
Size 32

counter a0

ROGUE_CR_JONES_PERF_SELECT0
Size 64

Address: 0x00008338

Access: read-write

Member of groups: jones_perf

63	62	61	60	59	58	57	56
reserved	BATCH_MAX (_) ...						

55	54	53	52	51	50	49	48

BATCH_MAX (_)

47	46	45	44	43	42	41	40
reserved		BATCH_MIN (_) ...					

39	38	37	36	35	34	33	32
BATCH_MIN (_)							

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved		MODE (_)	GROUP_SELECT (_)				

15	14	13	12	11	10	9	8
BIT_SELECT (_) ...							

7	6	5	4	3	2	1	0
BIT_SELECT (_) ...							

Name	MSB	LSB	Default
BATCH_MAX	61	48	0x3fff
BATCH_MIN	45	32	0
MODE	21	21	0
GROUP_SELECT	20	16	0
BIT_SELECT	15	0	0

BATCH_MAX
Size 14

this is the max batch number which will be counted in this group

BATCH_MIN
Size 14

this is the min batch number which will be counted in this group

MODE
Size 1

reduction mode, 0: bitwise increments, 1: unsigned count increment

GROUP_SELECT
Size 5

group select, see full PERF documentation for signals in each group

BIT_SELECT
Size 16

bit mask for enabled signals in group

ROGUE_CR_MARS_IDLE
Size 3

Address: 0x000008f8

Access: readonly

Member of groups: mars

7	6	5	4	3	2	1	0
-					MH_SYSARB0 (_)	CPU (_)	SOCIF (_) ...

Name	Type	MSB	LSB	Default
MH_SYSARB0	_	2	2	0x1
CPU	_	1	1	0x1
SOCIF	_	0	0	0x1

MH_SYSARB0
Size 1

SYSARB0 Module IDLE

CPU
Size 1

CPU Module IDLE

SOCIF
Size 1

SOCIF Module IDLE

/>

ROGUE_CR_META_BOOT
Size 1

Address: 0x00000bf8

Access: read-write

Member of groups: jones sidekick2 sidekick

7	6	5	4	3	2	1	0
-							MODE (_) ...

Name	Type	MSB	LSB	Default
MODE	_	0	0	0

MODE
Size 1

0 = Don't boot, 1 = Boot

ROGUE_CR_META_SP_MSLVCTRL0
Size: 32

Address: 0x00003080**Default:** N/A

Type: Software Only Register**Direction**: read-write**SCOPE:** GARTEN**SECURITY:** METASLVCTRL0

Register banks: jones

Kick pipeline: global

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)						AUTOINCR (_)	RD (_) ...

Name	MSB	LSB	Default	Description	Bank Filter
ADDR	31	2	0	32-bit byte address specifying the address at which the next read or write access should be made within the META core memory map.	
AUTOINCR	1	1	0	Selects auto-increment addressing mode when set to 1. The address specified in ADDR (bits 31-2) will be incremented after each transaction is transmitted by the slave port.	
RD	0	0	0	If written with the value 1 a read to the address specified (see below) will be issued and this bit will clear back to zero once the read transaction is transmitted by the slave port.	

ROGUE_CR_META_SP_MSLVCTRL0.ADDR

Size: 30

Type: Define

32-bit byte address specifying the address at which the next read or write access should be made within the META core memory map.

ROGUE_CR_META_SP_MSLVCTRL0.AUTOINCR

Size: 1

Type: Define

Selects auto-increment addressing mode when set to 1. The address specified in ADDR (bits 31-2) will be incremented after each transaction is transmitted by the slave port.

ROGUE_CR_META_SP_MSLVCTRL0.RD

Size: 1

Type: Define

If written with the value 1 a read to the address specified (see below) will be issued and this bit will clear back to zero once the read transaction is transmitted by the slave port.

ROGUE_CR_META_SP_MSLVCTRL1

Size: 32

Address: 0x000030c0**Default:** N/A

Type: Software Only Register**Direction**: read-write**SCOPE:** GARTEN

Register banks: jones

Kick pipeline: global

31	30	29	28	27	26	25	24
DEFERRTHREAD (_)	LOCK2_INTERLOCK (_)	ATOMIC_INTERLOCK (_)	*reserved*	GBLPORT_IDLE (_)	COREMEM_IDLE (_)	READY (_)	

23	22	21	20	19	18	17	16

DEFERRID (_)	DEFERR (_)	*reserved*	WR_ACTIVE (_)	*reserved*

15	14	13	12	11	10	9	8
reserved							

7	6	5	4	3	2	1	0
reserved		THREAD (_)		TRANS_SIZE (_)		BYTE_ROUND (_) ...	

Name	MSB	LSB	Default	Description	Bank Filter
DEFERR THREAD	31	30	0	Deferred bus error thread ID. (Read only)	
LOCK2_INTERLOCK	29	29	0	Slave interface LOCK2 interlock active (Read only)	
ATOMIC_INTERLOCK	28	28	0	Atomic inter-lock active in MMU arbiter (Read only)	
GBLPORT_IDLE	26	26	0	Global internal register access port idle (Read only)	
COREMEM_IDLE	25	25	0	Core memory update register idle (Read only)	
READY	24	24	0	Slave port ready to issue a further read or write request (Read only)	
DEFERRID	23	21	0	Deferred bus error code (Read only)	
DEFERR	20	20	0	This bit is set to '1' when a slave access generated a deferred bus error. Writing '0' to this bit clears this flag. Once this flag is set to '1', further bus errors would be ignored until it is cleared.	
WR_ACTIVE	18	18	0	If set means that a write is still in progress within the META core, else zero if write(s) have completed (Read only)	
THREAD	5	4	0	Specifies the thread identifier to be issued on read or write transactions within the META core.	
TRANS_SIZE	3	2	0	Selects the transaction size (number of byte lanes) generated within the META core for writes or reads. The following sizes are currently supported, 0 - 32-bit, 1 - 16-bit, and 2 - 8-bit.	
BYTE_ROUND	1	0	0	Byte routing/shift to be applied to data transfers performed on the MSLVDATAX and MSLVDATAT registers. Data will be duplicated in either direction so that 8-bit or 16-bit read or write operations can be performed using the lower part of the slave interface data bus.	

ROGUE_CR_META_SP_MSLVCTRL1.DEFERRTHREAD

Size: 2

Type: Define

Deferred bus error thread ID. (Read only)

ROGUE_CR_META_SP_MSLVCTRL1.LOCK2_INTERLOCK

Size: 1

Type: Define

Slave interface LOCK2 interlock active (Read only)

ROGUE_CR_META_SP_MSLVCTRL1.ATOMIC_INTERLOCK

Size: 1

Type: Define

Atomic inter-lock active in MMU arbiter (Read only)

ROGUE_CR_META_SP_MSLVCTRL1.GBLPORT_IDLE

Size: 1

Type: Define

Global internal register access port idle (Read only)

ROGUE_CR_META_SP_MSLVCTRL1.COREMEM_IDLE
Size: 1

Type: Define

Core memory update register idle (Read only)

ROGUE_CR_META_SP_MSLVCTRL1.READY
Size: 1

Type: Define

Slave port ready to issue a further read or write request (Read only)

ROGUE_CR_META_SP_MSLVCTRL1.DEFERRID
Size: 3

Type: Define

Deferred bus error code (Read only)

ROGUE_CR_META_SP_MSLVCTRL1.DEFERR
Size: 1

Type: Define

This bit is set to '1' when a slave access generated a deferred bus error. Writing '0' to this bit clears this flag. Once this flag is set to '1', further bus errors would be ignored until it is cleared.

ROGUE_CR_META_SP_MSLVCTRL1.WR_ACTIVE
Size: 1

Type: Define

If set means that a write is still in progress within the META core, else zero if write(s) have completed (Read only)

ROGUE_CR_META_SP_MSLVCTRL1.THREAD
Size: 2

Type: Define

Specifies the thread identifier to be issued on read or write transactions within the META core.

ROGUE_CR_META_SP_MSLVCTRL1.TRANS_SIZE
Size: 2

Type: Define

Selects the transaction size (number of byte lanes) generated within the META core for writes or reads. The following sizes are currently supported, 0 - 32-bit, 1 - 16-bit, and 2 - 8-bit.

ROGUE_CR_META_SP_MSLVCTRL1.BYTE_ROUND
Size: 2

Type: Define

Byte routing/shift to be applied to data transfers performed on the MSLVDATAX and MSLVDATAT registers. Data will be duplicated in either direction so that 8-bit or 16-bit read or write operations can be performed using the lower part of the slave interface data bus.

ROGUE_CR_META_SP_MSLVDATAT

Size: 32

Address: 0x00003040**Default:** N/A

Type: Software Only Register**Direction**: read-write**SCOPE:** GARTEN**SECURITY:** METASLVDATAT

Register banks: jones

Kick pipeline: global

31	30	29	28	27	26	25	24
MSLVDATAT (_) ...							

23	22	21	20	19	18	17	16
MSLVDATAT (_) ...							

15	14	13	12	11	10	9	8
MSLVDATAT (_) ...							

7	6	5	4	3	2	1	0
MSLVDATAT (_) ...							

Name	MSB	LSB	Default	Description	Bank Filter
MSLVDATAT	31	0	0	This register updates or returns the same value as MSLVDATAX. However each read/write transaction on this register also starts the corresponding transfer within the META Core	

ROGUE_CR_META_SP_MSLVDATAT.MSLVDATAT

Size: 32

Type: Define

This register updates or returns the same value as MSLVDATAX. However each read/write transaction on this register also starts the corresponding transfer within the META Core

ROGUE_CR_META_SP_MSLVDATAX

Size: 32

Address: 0x00003000**Default:** N/A

Type: Software Only Register**Direction**: read-write**SCOPE:** GARTEN

Register banks: jones

Kick pipeline: global

31	30	29	28	27	26	25	24
MSLVDATAX (_) ...							

23	22	21	20	19	18	17	16
MSLVDATAX (_) ...							

15	14	13	12	11	10	9	8
MSLVDATAX (_) ...							

7	6	5	4	3	2	1	0
MSLVDATAX (_) ...							

Name	MSB	LSB	Default	Description	Bank Filter
MSLVDATAX	31	0	0	This register holds the last data value read or written by the slave port	

ROGUE_CR_META_SP_MSLVDATAX.MSLVDATAX

Size: 32

Type: Define

This register holds the last data value read or written by the slave port

ROGUE_CR_META_SP_MSLVIRQENABLE

Size: 32

Address: 0x00003680**Default:** N/A

Type: Software Only Register**Direction**: read-write**SCOPE:** GARTEN

Register banks: jones

Kick pipeline: global

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved							

15	14	13	12	11	10	9	8
reserved							

7	6	5	4	3	2	1	0
reserved				EVENT1 (_)	EVENT0 (_)	*reserved*	

Name	MSB	LSB	Default	Description	Bank Filter
EVENT1	3	3	0	Enable Slave interrupt event 1 to raise an output interrupt.	
EVENT0	2	2	0	Enable Slave interrupt event 0 to raise an output interrupt.	

ROGUE_CR_META_SP_MSLVIRQENABLE.EVENT1

Size: 1

Type: Define

Enable Slave interrupt event 1 to raise an output interrupt.

ROGUE_CR_META_SP_MSLVIRQENABLE.EVENT0

Size: 1

Type: Define

Enable Slave interrupt event 0 to raise an output interrupt.

ROGUE_CR_META_SP_MSLVIRQLEVEL

Size: 32

Address: 0x000036c0**Default:** N/A

Type: Software Only Register**Direction**: read-write**SCOPE:** GARTEN

Register banks: jones

Kick pipeline: global

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved							

15	14	13	12	11	10	9	8
reserved							

7	6	5	4	3	2	1	0
reserved							MODE (_) ...

Name	MSB	LSB	Default	Description	Bank Filter
MODE	0	0	0	Level or edge mode for the META core output triggers.	

ROGUE_CR_META_SP_MSLVIRQSTATUS

Size: 32

Address: 0x00003640**Default:** N/A

Type: Software Only Register**Direction**: read-write**SCOPE:** GARTEN**SECURITY:** NONE

Register banks: jones

Kick pipeline: global

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved							

15	14	13	12	11	10	9	8
reserved							

7	6	5	4	3	2	1	0
reserved				TRIGVECT3 (_)	TRIGVECT2 (_)	*reserved*	

Name	MSB	LSB	Default	Description	Bank Filter
TRIGVECT3	3	3	0	IRQ event occurred due to vectoring to an event inside META core to the host (set trigger vector to 3). This status bit can be written with '0' to clear the IRQ event	
TRIGVECT2	2	2	0	IRQ event occurred due to vectoring to an event inside META core to the host (set trigger vector to 2). This status bit can be written with '0' to clear the IRQ event.	

ROGUE_CR_META_SP_MSLVIRQSTATUS.TRIGVECT3

Size: 1

Type: Define

IRQ event occurred due to vectoring to an event inside META core to the host (set trigger vector to 3). This status bit can be written with '0' to clear the IRQ event

ROGUE_CR_META_SP_MSLVIRQSTATUS.TRIGVECT2

Size: 1

Type: Define

IRQ event occurred due to vectoring to an event inside META core to the host (set trigger vector to 2). This status bit can be written with '0' to clear the IRQ event.

ROGUE_CR_MIPS_WRAPPER_IRQ_STATUS

Size 1

Address: 0x000008a8

Access: read-write

Member of groups: sidekick2 sidekick

7	6	5	4	3	2	1	0
-							EVENT (_) ...

This register contains the configuration options for the RGX firmware interrupts to HOST.

Name	Type	MSB	LSB	Default
EVENT	_	0	0	0

ROGUE_CR_MIPS_WRAPPER_NMI_ENABLE

Size 1

Address: 0x000008b8

Access: read-write

Member of groups: sidekick2 sidekick

7	6	5	4	3	2	1	0
-							EVENT (_) ...

This register contains the configuration options for the RGX firmware non-maskable interrupts to MIPS.

Name	Type	MSB	LSB	Default
EVENT	_	0	0	0

EVENT

Size 1

Allow RGX firmware to send non-maskable interrupts to MIPS

ROGUE_CR_MIPS_WRAPPER_NMI_EVENT

Size 1

Address: 0x000008c0

Access: writeonly

Member of groups: sidekick2 sidekick

7	6	5	4	3	2	1	0
-							TRIGGER (_) ...

This register contains the configuration options for the RGX firmware non-maskable interrupts to MIPS.

Name	Type	MSB	LSB	Default
TRIGGER	_	0	0	0

TRIGGER

Size 1

Issue a non-maskable interrupt to the MIPS SI_NMI pin from RGX firmware

ROGUE_CR_MMU_CBASE_MAPPING

Size: 29

Address: 0x0000e148**Default:** 0x0000000010000000

Type: Register**Direction**: read-write**External:** True**SCOPE:** VIRTUAL

Register banks: mmu_dv slc_dv slc

Kick pipeline: global

31	30	29	28	27	26	25	24
-			INVALID (_)	BASE_ADDR (_) ...			

23	22	21	20	19	18	17	16
BASE_ADDR (_) ...							

15	14	13	12	11	10	9	8
BASE_ADDR (_) ...							

7	6	5	4	3	2	1	0
BASE_ADDR (_) ...							

Page Catalogue base address read or write

Name	MSB	LSB	Default	Description	Bank Filter
INVALID	28	28	0x1	Invalid bit for PC base address of specified context. On a write SW specifies PC base address is valid (i.e. not invalid) when mapping it and can later invalidate by setting this bit. Indicates PC base address is invalid on a read	
BASE_ADDR	27	0	0	PC base address to be allocated to the specified context on a write. PC base address already allocated to the specified context on a read	

ROGUE_CR_MMU_CBASE_MAPPING.INVALID

Size: 1

Type: Define

Invalid bit for PC base address of specified context. On a write SW specifies PC base address is valid (i.e. not invalid) when mapping it and can later invalidate by setting this bit. Indicates PC base address is invalid on a read

ROGUE_CR_MMU_CBASE_MAPPING.BASE_ADDR

Size: 28

Type: Define**ALIGN:** 12

PC base address to be allocated to the specified context on a write. PC base address already allocated to the specified context on a read

ROGUE_CR_MMU_CBASE_MAPPING_CONTEXT

Size: 5

Address: 0x0000e140**Default:** 0

Type: Register**Direction**: read-write**Notify:** True**SCOPE:** VIRTUAL

Register banks: mmu_dv slc_dv slc

Kick pipeline: global

7	6	5	4	3	2	1	0
-			ID (_) ...				

Define context to read or write

Name	MSB	LSB	Default	Description	Bank Filter

ID	4	0	0		

ROGUE_CR_MMU_CBASE_MAPPING_CONTEXT.ID

Size: 5

Type: Define

ROGUE_CR_MMU_FAULT_STATUS

Size 64

Address: 0x0000e150

Access: read-write

Member of groups: slc3

63	62	61	60	59	58	57	56
ADDRESS (_) ...							

55	54	53	52	51	50	49	48
ADDRESS (_) ...							

47	46	45	44	43	42	41	40
ADDRESS (_) ...							

39	38	37	36	35	34	33	32
ADDRESS (_) ...							

31	30	29	28	27	26	25	24
ADDRESS (_)				CONTEXT (_) ...			

23	22	21	20	19	18	17	16
CONTEXT (_)				TAG_SB (_) ...			

15	14	13	12	11	10	9	8
TAG_SB (_)				REQ_ID (_) ...			

7	6	5	4	3	2	1	0
REQ_ID (_)		LEVEL (_)		RNW (_)	TYPE (_)		FAULT (_) ...

Indicates a page fault has occurred due to a non-Meta request and gives details of faulting request. Any write to this register will clear the contents and allow a subsequent fault to be reported

Name	MSB	LSB	Default
ADDRESS	63	28	0
CONTEXT	27	20	0
TAG_SB	19	12	0
REQ_ID	11	6	0
LEVEL	5	4	0
RNW	3	3	0
TYPE	2	1	0
FAULT	0	0	0

ADDRESS

Size 36

Virtual address

CONTEXT
Size 8

Context

TAG_SB
Size 8

Sideband tag

REQ_ID
Size 6

Requester ID - see ROGUE_bif3_pack/documentation for encoding

LEVEL
Size 2

MMU level that faulted: "00"=PT "01"=PD "10"=PC "11"=PC Base

RNW
Size 1

Indicates whether fault was caused by a read(1) or write(0) request

TYPE
Size 2

Type of fault: "00"=valid "10"=read-only "11"=pm/meta protected

FAULT
Size 1

Indicates a fault has occured

ROGUE_CR_MMU_FAULT_STATUS_META
Size: 64

Address: 0x0000e160**Default:** N/A

Type: Register**Direction**: read-only**Notify:** True**SCOPE:** VIRTUAL

Register banks: slc_dv slc

Kick pipeline: global

63	62	61	60	59	58	57	56
LEVEL (_)		REQ_ID (_)					

55	54	53	52	51	50	49	48
CONTEXT (_)							

47	46	45	44	43	42	41	40
ADDRESS (_) ...							

39	38	37	36	35	34	33	32

ADDRESS (_) ...

31	30	29	28	27	26	25	24
ADDRESS (_) ...							

23	22	21	20	19	18	17	16
ADDRESS (_) ...							

15	14	13	12	11	10	9	8
ADDRESS (_) ...							

7	6	5	4	3	2	1	0
ADDRESS (_)				RNW (_)	TYPE (_)		FAULT (_) ...

Indicates a page fault has occurred due to a Meta request and gives details of faulting request. Any write to this register will clear the contents and allow a subsequent fault to be reported

Name	MSB	LSB	Default	Description	Bank Filter
LEVEL	63	62	0	MMU level that faulted: "00"=PT "01"=PD "10"=PC "11"=PC Base	
REQ_ID	61	56	0	Requester ID - see BIF HW specification for details of the encoding	
CONTEXT	55	48	0	Context / Process Address Space ID (PASID)	
ADDRESS	47	4	0	48-bit Virtual Address (128-bit/16-byte aligned)	
RNW	3	3	0	Indicates whether fault was caused by a read(1) or write(0) request	
TYPE	2	1	0	Type of fault: "00"=valid "01"=FBCDC accessing Cache Coherent region "10"=read-only "11"=pm/meta protected	
FAULT	0	0	0	Indicates a fault has occured	

ROGUE_CR_MMU_FAULT_STATUS_META.LEVEL

Size: 2

Type: Define

MMU level that faulted: "00"=PT "01"=PD "10"=PC "11"=PC Base

ROGUE_CR_MMU_FAULT_STATUS_META.REQ_ID

Size: 6

Type: Define

Requester ID - see BIF HW specification for details of the encoding

ROGUE_CR_MMU_FAULT_STATUS_META.CONTEXT

Size: 8

Type: Define

Context / Process Address Space ID (PASID)

ROGUE_CR_MMU_FAULT_STATUS_META.ADDRESS

Size: 44

Type: Define

48-bit Virtual Address (128-bit/16-byte aligned)

ROGUE_CR_MMU_FAULT_STATUS_META.RNW

Size: 1

Type: Define

Indicates whether fault was caused by a read(1) or write(0) request

ROGUE_CR_MMU_FAULT_STATUS_META.TYPE

Size: 2

Type: Define

Type of fault: "00"=valid "01"=FBCDC accessing Cache Coherent region "10"=read-only "11"=pm/meta protected

ROGUE_CR_MMU_FAULT_STATUS_META.FAULT

Size: 1

Type: Define

Indicates a fault has occured

ROGUE_CR_MTS_BGCTX

Size 14

Address: 0x00000ba0

Access: readonly

Member of groups: jones mars

15	14	13	12	11	10	9	8
-	*reserved*						

7	6	5	4	3	2	1	0
DM_NONCOUNTED_SCHEDULE (_) ...							

This register contains the sideband data for the MTS internal background context registers

Name	Type	MSB	LSB	Default
DM_NONCOUNTED_SCHEDULE	_	7	0	0

DM_NONCOUNTED_SCHEDULE

Size 8

A 1 bit counter per DM for non-counted background request

ROGUE_CR_MTS_BGCTX_THREAD0_DM_ASSOC

Size 16

Address: 0x00000b30

Access: read-write

Member of groups: jones mars

15	14	13	12	11	10	9	8
DM_ASSOC (_) ...							

7	6	5	4	3	2	1	0
DM_ASSOC (_) ...							

This register is the DataMaster assocation for the background context of thread 0. Bit high represents DataMaster being permitted to run on the background context of thread 0.

Name	Type	MSB	LSB	Default
DM_ASSOC	_	15	0	0

DM_ASSOC
Size 16

DataMaster Association (Active High)

ROGUE_CR_MTS_BGCTX_THREAD1_DM_ASSOC
Size: 16

Address: 0x00000b38**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** GARTEN**SECURITY:** NONE

Register banks: jones

Kick pipeline: global

15	14	13	12	11	10	9	8
DM_ASSOC (_) ...							

7	6	5	4	3	2	1	0
DM_ASSOC (_) ...							

This register is the DataMaster assocation for the background context of thread 1. Bit high represents DataMaster being permitted to run on the background context of thread 1.

Name	MSB	LSB	Default	Description	Bank Filter
DM_ASSOC	15	0	0	DataMaster Association (Active High)	

ROGUE_CR_MTS_DM0_INTERRUPT_ENABLE
Size 32

Address: 0x00000b58

Access: read-write

Member of groups: jones mars

31	30	29	28	27	26	25	24
INT_ENABLE (_) ...							

23	22	21	20	19	18	17	16
INT_ENABLE (_) ...							

15	14	13	12	11	10	9	8
INT_ENABLE (_) ...							

7	6	5	4	3	2	1	0
INT_ENABLE (_) ...							

Interrupt enable status register for DataMaster 0

Name	Type	MSB	LSB	Default
INT_ENABLE	_	31	0	0

INT_ENABLE
Size 32

Interrupt Enable

ROGUE_CR_MTS_GARTEN_WRAPPER_CONFIG

Size 48

Address: 0x00000b50

Access: read-write

Member of groups: jones mars

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
reserved							

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved							

15	14	13	12	11	10	9	8
reserved							

7	6	5	4	3	2	1	0
reserved							IDLE_CTRL (IDLE_TYPE) ... = *MTS*

This register contains the configuration options for the Garten wrapper.

Name	Type	MSB	LSB	Default
IDLE_CTRL	IDLE_TYPE	0	0	MTS [0x1]

IDLE_TYPE

Size 1

Possible Values:

Name	Value /Range	Info
META	0 [0]	Top level idle signal controlled by META. IDLE high implies threads are complete and META can be powered down
MTS	1 [0x1]	Top level idle signal controlled by the MTS. IDLE high implies no tasks currently queued or running, css_clk_en may be taken low. css_clk_en must be taken high for MTS to recieve schedule requests.

ROGUE_CR_MTS_INTCTX

Size 30

Address: 0x00000b98

Access: readonly

Member of groups: jones mars

31	30	29	28	27	26	25	24
-	DM_HOST_SCHEDULE (_) ...						

23	22	21	20	19	18	17	16
DM_HOST_SCHEDULE (_)	*reserved*						

15	14	13	12	11	10	9	8
DM_TIMER_SCHEDULE (_)							

7	6	5	4	3	2	1	0
DM_INTERRUPT_SCHEDULE (_) ...							

This register contains the sideband data for the MTS internal interrupt context registers

Name	Type	MSB	LSB	Default
DM_HOST_SCHEDULE	_	29	22	0
DM_TIMER_SCHEDULE	_	15	8	0
DM_INTERRUPT_SCHEDULE	_	7	0	0

DM_INTERRUPT_SCHEDULE

Size 8

A 1 bit counter per DM for interrupt requests

DM_TIMER_SCHEDULE

Size 8

A 1 bit counter per DM for timer requests

DM_HOST_SCHEDULE

Size 8

A 1 bit counter per DM for host requests

ROGUE_CR_MTS_INTCTX_THREAD0_DM_ASSOC

Size 16

Address: 0x00000b40

Access: read-write

Member of groups: jones mars

15	14	13	12	11	10	9	8
DM_ASSOC (_) ...							

7	6	5	4	3	2	1	0
DM_ASSOC (_) ...							

This register is the DataMaster assocation for the interrupt context of thread 0. Bit high represents DataMaster being permitted to run on the interrupt context of thread 0.

Name	Type	MSB	LSB	Default
DM_ASSOC	_	15	0	0

DM_ASSOC

Size 16

DataMaster Association (Active High)

ROGUE_CR_MTS_INTCTX_THREAD1_DM_ASSOC

Size: 16

Address: 0x00000b48**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** GARTEN**SECURITY:** NONE

Register banks: jones

Kick pipeline: global

15	14	13	12	11	10	9	8
DM_ASSOC (_) ...							

7	6	5	4	3	2	1	0
DM_ASSOC (_) ...							

This register is the DataMaster assocation for the interrupt context of thread 1. Bit high represents DataMaster being permitted to run on the interrupt context of thread 1.

Name	MSB	LSB	Default	Description	Bank Filter
DM_ASSOC	15	0	0	DataMaster Association (Active High)	

ROGUE_CR_MTS_INTCTX_THREAD1_DM_ASSOC.DM_ASSOC

Size: 16

Type: Define

DataMaster Association (Active High)

ROGUE_CR_MTS_SCHEDULE

Size 9

Address: 0x00000b00

Access: read-write

Member of groups: jones mars

15	14	13	12	11	10	9	8
-							HOST (MTS_HOST_TYPE)

7	6	5	4	3	2	1	0
PRIORITY (MTS_PRIORITY_TYPE)		CONTEXT (MTS_CONTEXT_TYPE) = *BGCTX*	TASK (MTS_TASK_TYPE) = *NON_COUNTED*		DM (MTS_DM_TYPE) ...		

This register allows firmware tasks to be scheduled on the META (Garten) core.

Name	Type	MSB	LSB	Default
HOST	MTS_HOST_TYPE	8	8	0
PRIORITY	MTS_PRIORITY_TYPE	7	6	0
CONTEXT	MTS_CONTEXT_TYPE	5	5	BGCTX [0]
TASK	MTS_TASK_TYPE	4	4	NON_COUNTED [0]
DM	MTS_DM_TYPE	3	0	0

ROGUE_CR_MTS_SCHEDULE1

Size 9

Address: 0x00010b00

Access: read-write

Member of groups: jones mars

15	14	13	12	11	10	9	8
-							HOST (MTS_HOST_TYPE)

7	6	5	4	3	2	1	0

PRIORITY (MTS_PRIORITY_TYPE)	CONTEXT (MTS_CONTEXT_TYPE) = *BGCTX*	TASK (MTS_TASK_TYPE) = *NON_COUNTED*	DM (MTS_DM_TYPE) ...

This register allows firmware tasks to be scheduled on the META (Garten) core.

Name	Type	MSB	LSB	Default
HOST	MTS_HOST_TYPE	8	8	0
PRIORITY	MTS_PRIORITY_TYPE	7	6	0
CONTEXT	MTS_CONTEXT_TYPE	5	5	BGCTX [0]
TASK	MTS_TASK_TYPE	4	4	NON_COUNTED [0]
DM	MTS_DM_TYPE	3	0	0

ROGUE_CR_MTS_SCHEDULE_ENABLE

Size 8

Address: 0x00000bc8

Access: read-write

Member of groups: mars

7	6	5	4	3	2	1	0
MASK (_) ...							

This register is an active-high mask. When the bit is 0, the MTS_SCHEDULE kick from the corresponding Guest OS is silently discarded. This allows the FW to mask out a Guest OS in order to prevent denial-of-service style attacks.

Name	Type	MSB	LSB	Default
MASK	_	7	0	0xff

MASK

Size 8

ROGUE_CR_MULTICORE_GPU

Size 7

Address: 0x0000f300

Access: readonly

Member of groups: mars

7	6	5	4	3	2	1	0
-	CAPABILITY_FRAGMENT (_)	CAPABILITY_GEOMETRY (_)	CAPABILITY_COMPUTE (_)	CAPABILITY_PRIMARY (_)	ID (_) ...		

Name	Type	MSB	LSB	Default
CAPABILITY_FRAGMENT	_	6	6	0x1
CAPABILITY_GEOMETRY	_	5	5	0x1
CAPABILITY_COMPUTE	_	4	4	0x1
CAPABILITY_PRIMARY	_	3	3	0x1
ID	_	2	0	---

CAPABILITY_FRAGMENT

Size 1

Whether or not this core has fragment capability. A value of 1 means it has the capability.

CAPABILITY_GEOMETRY
Size 1

Whether or not this core has geometry capability. A value of 1 means it has the capability.

CAPABILITY_COMPUTE
Size 1

Whether or not this core has compute capability. A value of 1 means it has the capability.

CAPABILITY_PRIMARY
Size 1

If this field is set to one, then this core has job synchronisation capabilities (i.e. via its firmware scheduler) and can be used as a Primary core.

ID
Size 3

The ID number of the GPU within the multicore system

ROGUE_CR_MULTICORE_SYSTEM
Size 4

Address: 0x0000f308

Access: readonly

Member of groups: mars

7	6	5	4	3	2	1	0
-				GPU_COUNT (_) ...			

Multicore read-only count register.

Name	Type	MSB	LSB	Default
GPU_COUNT	_	3	0	0x1

GPU_COUNT
Size 4

The number of physical cores in this Primary-Secondary group of a multicore system. A value of zero is meaningless. This register is set via a top level pin.

ROGUE_CR_OS0_SCRATCH0
Size 32

Address: 0x00001a80

Access: read-write

Member of groups: mars

31	30	29	28	27	26	25	24
DATA (_) ...							

23	22	21	20	19	18	17	16
DATA (_) ...							

15	14	13	12	11	10	9	8

DATA (_) ...

7	6	5	4	3	2	1	0
DATA (_) ...							

Name	Type	MSB	LSB	Default
DATA	_	31	0	0

DATA
Size 32

ROGUE_CR_OS0_SCRATCH1
Size 32

Address: 0x00001a88

Access: read-write

Member of groups: mars

31	30	29	28	27	26	25	24
DATA (_) ...							

23	22	21	20	19	18	17	16
DATA (_) ...							

15	14	13	12	11	10	9	8
DATA (_) ...							

7	6	5	4	3	2	1	0
DATA (_) ...							

Name	Type	MSB	LSB	Default
DATA	_	31	0	0

DATA
Size 32

ROGUE_CR_OS0_SCRATCH2
Size 8

Address: 0x00001a90

Access: read-write

Member of groups: mars

7	6	5	4	3	2	1	0
DATA (_) ...							

Name	Type	MSB	LSB	Default
DATA	_	7	0	0

DATA
Size 8

ROGUE_CR_OS0_SCRATCH3

Size 8

Address: 0x00001a98

Access: read-write

Member of groups: mars

7	6	5	4	3	2	1	0
DATA (_) ...							

Name	Type	MSB	LSB	Default
DATA	_	7	0	0

DATA

Size 8

ROGUE_CR_PBE_INDIRECT

Size: 6

Address: 0x000083e0**Default:** 0

Type: Indirect Address Register**Direction**: read-write**GENERATE_RDONLY:** YES**SECURITY:** NONE

Register banks: pbe

7	6	5	4	3	2	1	0
-	ADDRESS (_) ...						

Defines which instance number of being read or written from

Name	MSB	LSB	Default	Description	Bank Filter
ADDRESS	5	0	---	Instance number	

ROGUE_CR_PBE_PERF

Size 5

Address: 0x00008478

Access: read-write

Member of groups: pbe_perf

7	6	5	4	3	2	1	0
-	CLR_3 (_)		CLR_2 (_)		CLR_1 (_)	CLR_0 (_)	CTRL_ENABLE (_) ...

Name	Type	MSB	LSB	Default
CLR_3	_	4	4	0
CLR_2	_	3	3	0
CLR_1	_	2	2	0
CLR_0	_	1	1	0
CTRL_ENABLE	_	0	0	0

CLR_3

Size 1

clear counter 3

CLR_2
Size 1

clear counter 2

CLR_1
Size 1

clear counter 1

CLR_0
Size 1

clear counter 0

CTRL_ENABLE
Size 1

enables the perf bus counters

ROGUE_CR_PBE_PERF_COUNTER_0
Size 32

Address: 0x000084b0

Access: readonly

Member of groups: pbe_perf

31	30	29	28	27	26	25	24
REG (_) ...							

23	22	21	20	19	18	17	16
REG (_) ...							

15	14	13	12	11	10	9	8
REG (_) ...							

7	6	5	4	3	2	1	0
REG (_) ...							

Name	Type	MSB	LSB	Default
REG	_	31	0	0

REG
Size 32

counter a0

ROGUE_CR_PBE_PERF_INDIRECT
Size 4

Address: 0x000083d8

Access: read-write

Member of groups: pbe_perf

7	6	5	4	3	2	1	0
-				ADDRESS (_) ...			

Name	MSB	LSB	Default
ADDRESS	3	0	---

ROGUE_CR_PBE_PERF_SELECT0

Size 64

Address: 0x00008480

Access: read-write

Member of groups: pbe_perf

63	62	61	60	59	58	57	56
reserved		BATCH_MAX (_) ...					

55	54	53	52	51	50	49	48
BATCH_MAX (_)							

47	46	45	44	43	42	41	40
reserved		BATCH_MIN (_) ...					

39	38	37	36	35	34	33	32
BATCH_MIN (_)							

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved	MODE (_)		GROUP_SELECT (_)				

15	14	13	12	11	10	9	8
BIT_SELECT (_) ...							

7	6	5	4	3	2	1	0
BIT_SELECT (_) ...							

Name	Type	MSB	LSB	Default
BATCH_MAX	_	61	48	0x3fff
BATCH_MIN	_	45	32	0
MODE	_	21	21	0
GROUP_SELECT	_	20	16	0
BIT_SELECT	_	15	0	0

BATCH_MAX

Size 14

this is the max batch number which will be counted in this group

BATCH_MIN
Size 14

this is the min batch number which will be counted in this group

MODE
Size 1

reduction mode, 0: bitwise increments, 1: unsigned count increment

GROUP_SELECT
Size 5

group select, see full PERF documentation for signals in each group

BIT_SELECT
Size 16

bit mask for enabled signals in group

ROGUE_CR_PERF_3D_CYCLE
Size 32

Address: 0x00006028

Access: readonly

Member of groups: jones mars

31	30	29	28	27	26	25	24
COUNT (_) ...							

23	22	21	20	19	18	17	16
COUNT (_) ...							

15	14	13	12	11	10	9	8
COUNT (_) ...							

7	6	5	4	3	2	1	0
COUNT (_) ...							

Name	Type	MSB	LSB	Default
COUNT	_	31	0	0

COUNT
Size 32

The number of cycles spent in 3D phases

ROGUE_CR_PERF_TA_CYCLE
Size 32

Address: 0x00006020

Access: readonly

Member of groups: jones mars

31	30	29	28	27	26	25	24
COUNT (_) ...							

23	22	21	20	19	18	17	16
COUNT (_) ...							

15	14	13	12	11	10	9	8
COUNT (_) ...							

7	6	5	4	3	2	1	0
COUNT (_) ...							

Name	Type	MSB	LSB	Default
COUNT	_	31	0	0

COUNT

Size 32

The number of cycles spent in TA phases

ROGUE_CR_PERF_TA_OR_3D_CYCLE

Size 32

Address: 0x00006038

Access: readonly

Member of groups: jones mars

31	30	29	28	27	26	25	24
COUNT (_) ...							

23	22	21	20	19	18	17	16
COUNT (_) ...							

15	14	13	12	11	10	9	8
COUNT (_) ...							

7	6	5	4	3	2	1	0
COUNT (_) ...							

Name	Type	MSB	LSB	Default
COUNT	_	31	0	0

COUNT

Size 32

The number of cycles spent in TA phases or 3D phases

ROGUE_CR_POWER_ESTIMATE_RESULT

Size 32

Address: 0x00006328

Access: read-write

Member of groups: sidekick2 sidekick

31	30	29	28	27	26	25	24
VALUE (_) ...							

23	22	21	20	19	18	17	16
VALUE (_) ...							

15	14	13	12	11	10	9	8
VALUE (_) ...							

7	6	5	4	3	2	1	0
VALUE (_) ...							

Power Estimate Result. This represents the estimation of the total system power usage.

Name	Type	MSB	LSB	Default
VALUE	_	31	0	---

VALUE
Size 32

ROGUE_CR_RASTERISATION_PERF
Size 5

Address: 0x00007700

Access: read-write

Member of groups: rasterisation_perf

7	6	5	4	3	2	1	0
-			CLR_3 (_)	CLR_2 (_)	CLR_1 (_)	CLR_0 (_)	CTRL_ENABLE (_) ...

Name	Type	MSB	LSB	Default
CLR_3	_	4	4	0
CLR_2	_	3	3	0
CLR_1	_	2	2	0
CLR_0	_	1	1	0
CTRL_ENABLE	_	0	0	0

CLR_3
Size 1

clear counter 3

CLR_2
Size 1

clear counter 2

CLR_1
Size 1

clear counter 1

CLR_0
Size 1

clear counter 0

CTRL_ENABLE
Size 1

enables the perf bus counters

ROGUE_CR_RASTERISATION_PERF_COUNTER_0
Size 32

Address: 0x00007750

Access: readonly

Member of groups: rasterisation_perf

31	30	29	28	27	26	25	24
REG (_) ...							

23	22	21	20	19	18	17	16
REG (_) ...							

15	14	13	12	11	10	9	8
REG (_) ...							

7	6	5	4	3	2	1	0
REG (_) ...							

Name	Type	MSB	LSB	Default
REG	_	31	0	0

REG
Size 32

counter a0

ROGUE_CR_RASTERISATION_PERF_INDIRECT
Size 4

Address: 0x00008318

Access: read-write

Member of groups: rasterisation_perf

7	6	5	4	3	2	1	0
-				ADDRESS (_) ...			

Name	MSB	LSB	Default
ADDRESS	3	0	---

ROGUE_CR_RASTERISATION_PERF_SELECT0
Size 64

Address: 0x00007708

Access: read-write

Member of groups: rasterisation_perf

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
reserved							

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved		MODE (_)	GROUP_SELECT (_)				

15	14	13	12	11	10	9	8
BIT_SELECT (_) ...							

7	6	5	4	3	2	1	0
BIT_SELECT (_) ...							

Name	Type	MSB	LSB	Default
MODE	_	21	21	0
GROUP_SELECT	_	20	16	0
BIT_SELECT	_	15	0	0

MODE
Size 1

reduction mode, 0: bitwise increments, 1: unsigned count increment

GROUP_SELECT
Size 5

group select, see full PERF rasterisation documentation for signals in each group

BIT_SELECT
Size 16

bit mask for enabled signals in group

ROGUE_CR_SAFETY_EVENT_ENABLE
Size 32

Address: 0x0000f390

Access: read-write

Member of groups: mars

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved							

15	14	13	12	11	10	9	8
reserved							

7	6	5	4	3	2	1	0
GPU_LOCKUP (_)	CPU_PAGE_FAULT (_)	SAFE_COMPUTE_FAIL (_)	WATCHDOG_TIMEOUT (_)	TRP_FAIL (_)	FAULT_FW (_)	FAULT_GPU (_)	GPU_PAGE_FAULT (_) ...

This register is used to enable Safety mechanism interrupts directly to the host Writing a '1' to a bit field enables the relevant safety event

Name	Type	MSB	LSB	Default
GPU_LOCKUP	_	7	7	---
CPU_PAGE_FAULT	_	6	6	---
SAFE_COMPUTE_FAIL	_	5	5	---
WATCHDOG_TIMEOUT	_	4	4	---
TRP_FAIL	_	3	3	---
FAULT_FW	_	2	2	---
FAULT_GPU	_	1	1	---
GPU_PAGE_FAULT	_	0	0	---

GPU_PAGE_FAULT

Size 1

Set if a GPU page fault has been detected.

FAULT_GPU

Size 1

Set if a parity failure has been detected in GPU

FAULT_FW

Size 1

Set if a parity failure has been detected in FW processor

TRP_FAIL

Size 1

Set if TRP checksum check has failed

WATCHDOG_TIMEOUT

Size 1

Set if HW watchdog timer has timed out

SAFE_COMPUTE_FAIL

Size 1

Set if workgroup protection checksum comparison has failed

CPU_PAGE_FAULT
Size 1

Set if a CPU page fault has been detected.

GPU_LOCKUP
Size 1

Set if GPU has locked up

ROGUE_CR_SCRATCH1
Size 32

Address: 0x00001a08

Access: read-write

Member of groups: mars

31	30	29	28	27	26	25	24
DATA (_) ...							

23	22	21	20	19	18	17	16
DATA (_) ...							

15	14	13	12	11	10	9	8
DATA (_) ...							

7	6	5	4	3	2	1	0
DATA (_) ...							

Internal 'scratch' register for debug use by the firmware.

Name	Type	MSB	LSB	Default
DATA	_	31	0	0

DATA
Size 32

ROGUE_CR_SCRATCH11
Size 32

Address: 0x00001a58

Access: read-write

Member of groups: mars

31	30	29	28	27	26	25	24
DATA (_) ...							

23	22	21	20	19	18	17	16
DATA (_) ...							

15	14	13	12	11	10	9	8
DATA (_) ...							

7	6	5	4	3	2	1	0
DATA (_) ...							

Internal 'scratch' register for debug use by the firmware.

Name	Type	MSB	LSB	Default
DATA	_	31	0	0

DATA
Size 32

ROGUE_CR_SCRATCH14
Size 32

Address: 0x00001a70

Access: read-write

Member of groups: mars

31	30	29	28	27	26	25	24
DATA (_) ...							

23	22	21	20	19	18	17	16
DATA (_) ...							

15	14	13	12	11	10	9	8
DATA (_) ...							

7	6	5	4	3	2	1	0
DATA (_) ...							

Internal 'scratch' register for debug use by the firmware.

Name	Type	MSB	LSB	Default
DATA	_	31	0	0

DATA
Size 32

ROGUE_CR_SIDEKICK_IDLE
Size 7

Address: 0x000003c8

Access: readonly

Member of groups: sidekick2 sidekick

7	6	5	4	3	2	1	0
-	FB_CDC (_)	MMU (_)	BIF128 (_)	TLA (_)	GARTEN (_)	HOSTIF (_)	SOCIF (_) ...

Name	Type	MSB	LSB	Default
FB_CDC	_	6	6	0x1
MMU	_	5	5	0x1
BIF128	_	4	4	0x1
TLA	_	3	3	0x1
GARTEN	_	2	2	0x1
HOSTIF	_	1	1	0x1

SOCIF	_	0	0	0x1

FB_CDC
Size 1

FB CDC Module IDLE

MMU
Size 1

MMU Module IDLE

BIF128
Size 1

BIF128 Module IDLE

TLA
Size 1

TLA Module IDLE

GARTEN
Size 1

GARTEN Module IDLE

HOSTIF
Size 1

HOSTIF Module IDLE

SOCIF
Size 1

SOCIF Module IDLE

ROGUE_CR_SLC3_CTRL_MISC
Size 9

Address: 0x0000e200

Access: read-write

Member of groups: slc3

15	14	13	12	11	10	9	8
-							WRITE_COMBINER (_)

7	6	5	4	3	2	1	0
reserved					ADDR_DECODE_MODE (DECODE_MODE) ... = *LINEAR*		

SLC Control registers

Name	MSB	LSB	Default
WRITE_COMBINER	8	8	0x1
ADDR_DECODE_MODE	2	0	LINEAR [0]

DECODE_MODE

Size 3

Possible Values:

Name	Value /Range	Info
LINEAR	0 [0]	Addresses are interleaved between Cache Banks on a Cacheline boundary
IN_PAGE_HASH	1 [0x1]	Addresses interleaved between Cache Banks using an XOR hash of the address bits below the 4KB page granularity
FIXED_PVR_HASH	2 [0x2]	Addresses interleaved between Cache Banks using an XOR hash of the upper address bits
SCRAMBLE_PVR_HASH	3 [0x3]	Addresses interleaved between Cache Banks using an XOR hash of the upper address bits in combination with the scramble bits register
WEAVED_HASH	4 [0x4]	Addresses interleaved between Cache Groups using a weaved XOR hash of address bits

WRITE_COMBINER

Size 1

Controls whether the write combiner is enabled or not

ROGUE_CR_SLC3_IDLE

Size 20

Address: 0x0000e228

Access: readonly

Member of groups: slc3

23	22	21	20	19	18	17	16
-				ORDERQ_DUST2 (_)		MMU (_)	RDI (_)

15	14	13	12	11	10	9	8
IMGBV4 (_)				CACHE_BANKS (_) ...			

7	6	5	4	3	2	1	0
CACHE_BANKS (_)				ORDERQ_DUST (_)		ORDERQ_JONES (_)	XBAR (_) ...

Name	MSB	LSB	Default
ORDERQ_DUST2	19	18	0x3
MMU	17	17	0x1
RDI	16	16	0x1
IMGBV4	15	12	0xf
CACHE_BANKS	11	4	0xff
ORDERQ_DUST	3	2	0x3
ORDERQ_JONES	1	1	0x1
XBAR	0	0	0x1

ORDERQ_DUST2

Size 2

Per-Dust Order Queue Module IDLEs for instances 2-3

MMU
Size 1

MMU Module IDLE

RDI
Size 1

Return Data Interface Module IDLE

IMGBV4
Size 4

IMG Bus v4 Module IDLEs

CACHE_BANKS
Size 8

Cache Bank IDLEs

ORDERQ_DUST
Size 2

Per-Dust Order Queue Module IDLEs for instances 0-1

ORDERQ_JONES
Size 1

Jones Order Queue Module IDLE

XBAR
Size 1

CrossBar Module IDLE

ROGUE_CR_SLC3_SCRAMBLE
Size 64

Address: 0x0000e208

Access: read-write

Member of groups: slc3

63	62	61	60	59	58	57	56
BITS (_) ...							

55	54	53	52	51	50	49	48
BITS (_) ...							

47	46	45	44	43	42	41	40
BITS (_) ...							

39	38	37	36	35	34	33	32
BITS (_) ...							

31	30	29	28	27	26	25	24
BITS (_) ...							

23	22	21	20	19	18	17	16
BITS (_) ...							

15	14	13	12	11	10	9	8
BITS (_) ...							

7	6	5	4	3	2	1	0
BITS (_) ...							

SLC Control registers

Name	MSB	LSB	Default
BITS	63	0	0

ROGUE_CR_SLC3_SCRAMBLE2

Size 64

Address: 0x0000e210

Access: read-write

Member of groups: slc3

63	62	61	60	59	58	57	56
BITS (_) ...							

55	54	53	52	51	50	49	48
BITS (_) ...							

47	46	45	44	43	42	41	40
BITS (_) ...							

39	38	37	36	35	34	33	32
BITS (_) ...							

31	30	29	28	27	26	25	24
BITS (_) ...							

23	22	21	20	19	18	17	16
BITS (_) ...							

15	14	13	12	11	10	9	8
BITS (_) ...							

7	6	5	4	3	2	1	0
BITS (_) ...							

SLC Control registers

Name	MSB	LSB	Default
BITS	63	0	0

BITS

Size 64

Pattern of bits used to determine the Cache Bank in Address Decode mode 0x3. The actual Cache Bank to use is determined by indexing into the Scramble Bits, see the SLC HW specification for more details

ROGUE_CR_SLC3_SCRAMBLE3

Size 64

Address: 0x0000e218

Access: read-write

Member of groups: slc3

63	62	61	60	59	58	57	56
BITS (_) ...							

55	54	53	52	51	50	49	48
BITS (_) ...							

47	46	45	44	43	42	41	40
BITS (_) ...							

39	38	37	36	35	34	33	32
BITS (_) ...							

31	30	29	28	27	26	25	24
BITS (_) ...							

23	22	21	20	19	18	17	16
BITS (_) ...							

15	14	13	12	11	10	9	8
BITS (_) ...							

7	6	5	4	3	2	1	0
BITS (_) ...							

SLC Control registers

Name	MSB	LSB	Default
BITS	63	0	0

BITS

Size 64

Pattern of bits used to determine the Cache Bank in Address Decode mode 0x3. The actual Cache Bank to use is determined by indexing into the Scramble Bits, see the SLC HW specification for more details

ROGUE_CR_SLC3_SCRAMBLE4

Size 64

Address: 0x0000e260

Access: read-write

Member of groups: slc3

63	62	61	60	59	58	57	56
BITS (_) ...							

55	54	53	52	51	50	49	48

BITS (_) ...							

47	46	45	44	43	42	41	40
BITS (_) ...							

39	38	37	36	35	34	33	32
BITS (_) ...							

31	30	29	28	27	26	25	24
BITS (_) ...							

23	22	21	20	19	18	17	16
BITS (_) ...							

15	14	13	12	11	10	9	8
BITS (_) ...							

7	6	5	4	3	2	1	0
BITS (_) ...							

SLC Control registers

Name	MSB	LSB	Default
BITS	63	0	0

BITS

Size 64

Pattern of bits used to determine the Cache Bank in Address Decode mode 0x3. The actual Cache Bank to use is determined by indexing into the Scramble Bits, see the SLC HW specification for more details

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ROGUE_CR_SLC_CTRL_BYPASS

Size 60

Address: 0x00003828

Access: read-write

Member of groups: tpu_mcu_l0 hub sidekick ta rasterisation bifpmcache slc

63	62	61	60	59	58	57	56
-				REQ_TFBC_COMP_ZLS (_)	REQ_TFBC_DECOMP_ZLS_HEADER (_)	REQ_TFBC_DECOMP_TCU_HEADER (_)	REQ_TFBC_DECOMP_ZLS_DATA (_)

55	54	53	52	51	50	49	48
REQ_TFBC_DECOMP_TCU_DATA (_)	REQ_TFBC_COMP_PBE (_)	REQ_TCU_DM_COMPUTE (_)	PDSRW_NOLINEFILL (_)	PBE_NOLINEFILL (_)	*reserved*	REQ_IPF_RREQ (_)	REQ_IPF_CREQ (_)

47	46	45	44	43	42	41	40
REQ_IPF_PREQ (_)	REQ_IPF_DBSC (_)	REQ_TCU (_)	REQ_PBE (_)	REQ_ISP (_)	REQ_PM (_)	*reserved*	REQ_CDM (_)

39	38	37	36	35	34	33	32
REQ_TSPF_PDS_STATE (_)	REQ_TSPF_DB (_)	REQ_TSPF_VTX_VAR (_)	REQ_VDM (_)	REQ_TA_PSG_STREAM (_)	REQ_TA_PSG_REGION (_)	REQ_TA_VCE (_)	REQ_TA_PPP (_)

31	30	29	28	27	26	25	24
reserved	DM_PM_ALIST (_)	DM_PB_TE (_)	DM_PB_VCE (_)	*reserved*		REQ_IPF_CPF (_)	REQ_TPU (_)

23	22	21	20	19	18	17	16

reserved	BYP_CC_N (_)	BYP_CC (_)	REQ_MCU (_)	REQ_PDS (_)	REQ_TPF (_)	REQ_TA_TPC (_)

15	14	13	12	11	10	9	8
reserved	REQ_USC (_)	REQ_META (_)	REQ_HOST (_)	REQ_MMU_PT (_)	REQ_MMU_PD (_)	REQ_MMU_PC (_)	*reserved*

7	6	5	4	3	2	1	0
reserved		DM_HOST_META (_)	DM_MMU (_)	DM_COMPUTE (_)	DM_PIXEL (_)	DM_TA (_)	ALL (_) ...

SLC Bypass control

Name	Type	MSB	LSB	Default
REQ_TFBC_COMP_ZLS	_	59	59	0
REQ_TFBC_DECOMP_ZLS_HEADER	_	58	58	0
REQ_TFBC_DECOMP_TCU_HEADER	_	57	57	0
REQ_TFBC_DECOMP_ZLS_DATA	_	56	56	0
REQ_TFBC_DECOMP_TCU_DATA	_	55	55	0
REQ_TFBC_COMP_PBE	_	54	54	0
REQ_TCU_DM_COMPUTE	_	53	53	0
PDSRW_NOLINEFILL	_	52	52	0
PBE_NOLINEFILL	_	51	51	0
REQ_IPF_RREQ	_	49	49	0
REQ_IPF_CREQ	_	48	48	0
REQ_IPF_PREQ	_	47	47	0
REQ_IPF_DBSC	_	46	46	0
REQ_TCU	_	45	45	0x1
REQ_PBE	_	44	44	0x1
REQ_ISP	_	43	43	0x1
REQ_PM	_	42	42	0x1
REQ_CDM	_	40	40	0x1
REQ_TSPF_PDS_STATE	_	39	39	0
REQ_TSPF_DB	_	38	38	0
REQ_TSPF_VTX_VAR	_	37	37	0
REQ_VDM	_	36	36	0x1
REQ_TA_PSG_STREAM	_	35	35	0x1
REQ_TA_PSG_REGION	_	34	34	0x1
REQ_TA_VCE	_	33	33	0x1
REQ_TA_PPP	_	32	32	0x1
DM_PM_ALIST	_	30	30	0
DM_PB_TE	_	29	29	0
DM_PB_VCE	_	28	28	0
REQ_IPF_CPF	_	25	25	0
REQ_TPU	_	24	24	0
BYP_CC_N	_	21	21	0
BYP_CC	_	20	20	0
REQ_MCU	_	19	19	0
REQ_PDS	_	18	18	0
REQ_TPF	_	17	17	0
REQ_TA_TPC	_	16	16	0
REQ_USC	_	14	14	0
REQ_META	_	13	13	0

REQ_HOST	_	12	12	0
REQ_MMU_PT	_	11	11	0
REQ_MMU_PD	_	10	10	0
REQ_MMU_PC	_	9	9	0
DM_HOST_META	_	5	5	0
DM_MMU	_	4	4	0
DM_COMPUTE	_	3	3	0
DM_PIXEL	_	2	2	0
DM_TA	_	1	1	0
ALL	_	0	0	0

REQ_TFBC_COMP_ZLS
Size 1

Bypass SLC for TFBC_COMP ZLS requestor

REQ_TFBC_DECOMP_ZLS_HEADER
Size 1

Bypass SLC for TFBC_DECOMP ZLS Header requestor

REQ_TFBC_DECOMP_TCU_HEADER
Size 1

Bypass SLC for TFBC_DECOMP TCU Header requestor

REQ_TFBC_DECOMP_ZLS_DATA
Size 1

Bypass SLC for TFBC_DECOMP ZLS Delta requestor

REQ_TFBC_DECOMP_TCU_DATA
Size 1

Bypass SLC for TFBC_DECOMP TCU Delta requestor

REQ_TFBC_COMP_PBE
Size 1

Bypass SLC for TFBC_COMP PBE requestor

REQ_TCU_DM_COMPUTE
Size 1

Bypass SLC when DM is COMPUTE for TCU requests

PDSRW_NOLINEFILL
Size 1

PDSRW nolinefill set

PBE_NOLINEFILL
Size 1

PBE nolinefill set

REQ_IPF_RREQ
Size 1

Bypass SLC for IPF (RREQ) requestor

REQ_IPF_CREQ
Size 1

Bypass SLC for IPF (CREQ) requestor

REQ_IPF_PREQ
Size 1

Bypass SLC for IPF (PREQ) requestor

REQ_IPF_DBSC
Size 1

Bypass SLC for IPF (DBSC) requestor

REQ_TCU
Size 1

Bypass SLC for TCU requests

REQ_PBE
Size 1

Bypass SLC for PBE requestor

REQ_ISP
Size 1

Bypass SLC for the ISP requestor

REQ_PM
Size 1

Bypass SLC for the PM requestor

REQ_CDM
Size 1

Bypass SLC for the CDM requestor

REQ_TSPF_PDS_STATE
Size 1

Bypass SLC for the TSPF PDS STATE requestor

REQ_TSPF_DB
Size 1

Bypass SLC for the TSPF DB requestor

REQ_TSPF_VTX_VAR
Size 1

Bypass SLC for the TSPF VTX VAR requestor

REQ_VDM
Size 1

Bypass SLC for VDM requestor

REQ_TA_PSG_STREAM
Size 1

Bypass SLC for the TA (PSG Stream) requestor

REQ_TA_PSG_REGION
Size 1

Bypass SLC for the TA (PSG Region) requestor

REQ_TA_VCE
Size 1

Bypass SLC for the TA (VCE) requestor

REQ_TA_PPP
Size 1

Bypass SLC for the TA (PPP) requestor

DM_PM_ALIST
Size 1

Bypass SLC for the PM_ALIST data master

DM_PB_TE
Size 1

Bypass SLC for the PB_TE data master

DM_PB_VCE
Size 1

Bypass SLC for the PB_VCE data master

REQ_IPF_CPF
Size 1

Bypass SLC for IPF (CPF) requestor

REQ_TPU
Size 1

Bypass SLC for TPU requests coming from the MCU requestor

BYP_CC_N
Size 1

Bypass SLC when Cache Coherency bit is not set

BYP_CC
Size 1

Bypass SLC when Cache Coherency bit is set

REQ_MCU
Size 1

Bypass SLC for the MCU requestor

REQ_PDS
Size 1

Bypass SLC for the PDS requestor

REQ_TPF
Size 1

Bypass SLC for the TPF requestor

REQ_TA_TPC
Size 1

Bypass SLC for the TA (Tail Pointer Cache data) requestor

REQ_USC
Size 1

Bypass SLC for the USC requestor

REQ_META
Size 1

Bypass SLC for the META requestor

REQ_HOST
Size 1

Bypass SLC for the Host requestor

REQ_MMU_PT
Size 1

Bypass SLC for the MMU requestor (Page Table data)

REQ_MMU_PD
Size 1

Bypass SLC for the MMU requestor (Page Directory data)

REQ_MMU_PC
Size 1

Bypass SLC for the MMU requestor (Page Catalogue data)

DM_HOST_META
Size 1

Bypass SLC the HOST/META data master

DM_MMU
Size 1

Bypass SLC the MMU data master

DM_COMPUTE
Size 1

Bypass SLC the COMPUTE data master

DM_PIXEL
Size 1

Bypass SLC for the PIXEL data master

DM_TA
Size 1

Bypass SLC for the TA group which includes VERTEX, TESSELLATOR & STREAM_OUT data masters

ALL
Size 1

Bypass SLC for all requesters

ROGUE_CR_SLC_CTRL_MISC
Size 64

Address: 0x00003800

Access: read-write

Member of groups: slc2 slc

63	62	61	60	59	58	57	56
SCRAMBLE_BITS (_) ...							

55	54	53	52	51	50	49	48
SCRAMBLE_BITS (_) ...							

47	46	45	44	43	42	41	40
SCRAMBLE_BITS (_) ...							

39	38	37	36	35	34	33	32
SCRAMBLE_BITS (_)							

31	30	29	28	27	26	25	24
reserved						TAG_ID_LIMIT_CONTROL (_)	LAZYWB_OVERRIDE (_)

23	22	21	20	19	18	17	16
ADDR_DECODE_MODE (DECODE_MODE) = *INTERLEAVED_64_BYTE*							

15	14	13	12	11	10	9	8
reserved							PAUSE (_)

7	6	5	4	3	2	1	0
reserved				RESP_PRIORITY (_)	ENABLE_LINE_USE_LIMIT (_)	ENABLE_PSG_HAZARD_CHECK (_)	BYPASS_BURST_COMBINER (_) ...

SLC control registers

Name	Type	MSB	LSB	Default
SCRAMBLE_BITS	_	63	32	0
TAG_ID_LIMIT_CONTROL	_	25	25	0
LAZYWB_OVERRIDE	_	24	24	0
ADDR_DECODE_MODE	DECODE_MODE	23	16	INTERLEAVED_64_BYTE [0]
PAUSE	_	8	8	0
RESP_PRIORITY	_	3	3	0
ENABLE_LINE_USE_LIMIT	_	2	2	0
ENABLE_PSG_HAZARD_CHECK	_	1	1	0x1
BYPASS_BURST_COMBINER	_	0	0	0x1

DECODE_MODE

Size 8

Possible Values:

Name	Value /Range	Info
INTERLEAVED_64_BYTE	0 [0]	Addresses interleaved between cache banks on a 64byte boundary
INTERLEAVED_128_BYTE	1 [0x1]	Addresses interleaved between cache banks on a 128byte boundary
SIMPLE_HASH1	16 [0x10]	Addresses interleaved between cache banks using a simple XOR hash of bits 6 & 7 with 3 upper address bits
SIMPLE_HASH2	17 [0x11]	Addresses interleaved between cache banks using a simple XOR hash of bits 6 & 7 with 5 upper address bits
PVR_HASH1	32 [0x20]	Addresses interleaved between cache banks using an XOR hash of the upper address bits
PVR_HASH2_SCRAMBLE	33 [0x21]	Addresses interleaved between cache banks using an XOR hash of the upper address bits in combination with the scramble bits register

SCRAMBLE_BITS

Size 32

Pattern of bits used to determine the Cache Bank in Address Decode mode 0x21. The actual Cache Bank to use is determined by indexing into the 32 Scramble Bits using the 5 LSB's of the Hash result and then XORing this with Bit 6 of the incoming address to give a single bit result

TAG_ID_LIMIT_CONTROL

Size 1

Controls the number of external memory tag IDs available to SLC

LAZYWB_OVERRIDE

Size 1

Override cache policy of requests with lazy write back to write back

PAUSE
Size 1

Pause the SLC

RESP_PRIORITY
Size 1

Priority setting between Hit and Miss on return response. Default is round robin and set to 1 if miss needs priority over hit

ENABLE_LINE_USE_LIMIT
Size 1

Enable the use of cache line limits

ENABLE_PSG_HAZARD_CHECK
Size 1

Enable the hazard checking of PSG writes, only turn off if strict write ordering is guaranteed in the memory fabric

BYPASS_BURST_COMBINER
Size 1

Disable the burst combiner on the external memory interface

ROGUE_CR_SLC_IDLE
Size 10

Address: 0x00003898

Access: readonly

Member of groups: slc2 slc

15	14	13	12	11	10	9	8
-						*reserved*	

7	6	5	4	3	2	1	0
IMGBV4 (_)	CACHE_BANKS (_)	RBOFIFO (_)	FRC_CONV (_)	VXE_CONV (_)	VXD_CONV (_)	BIF1_CONV (_)	CBAR (_) ...

Name	Type	MSB	LSB	Default
IMGBV4	_	7	7	0x1
CACHE_BANKS	_	6	6	0x1
RBOFIFO	_	5	5	0x1
FRC_CONV	_	4	4	0x1
VXE_CONV	_	3	3	0x1
VXD_CONV	_	2	2	0x1
BIF1_CONV	_	1	1	0x1
CBAR	_	0	0	0x1

IMGBV4
Size 1

IMG Bus v4 Module IDLE

CACHE_BANKS
Size 1

Cache Bank IDLEs

RBOFIFO
Size 1

Read Burst Order FIFO Module IDLE

FRC_CONV
Size 1

FRC Module IDLE

VXE_CONV
Size 1

Video Encode Converter Module IDLE

VXD_CONV
Size 1

Video Decode Converter Module IDLE

BIF1_CONV
Size 1

BIF128->256 Converter Module IDLE

CBAR
Size 1

CrossBar Module IDLE

ROGUE_CR_SLC_STATUS1
Size 64

Address: 0x00003870

Access: readonly

Member of groups: slc2 slc

63	62	61	60	59	58	57	56
PAUSED (_)	*reserved*						

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
reserved						READS1 (_) ...	

39	38	37	36	35	34	33	32
READS1 (_)							

31	30	29	28	27	26	25	24

reserved						READS0 (_) ...	

23	22	21	20	19	18	17	16
READS0 (_)							

15	14	13	12	11	10	9	8
READS1_EXT (_)							

7	6	5	4	3	2	1	0
READS0_EXT (_) ...							

Current status of the SLC

Name	Type	MSB	LSB	Default
PAUSED	_	63	63	---
READS1	_	41	32	---
READS0	_	25	16	---
READS1_EXT	_	15	8	---
READS0_EXT	_	7	0	---

PAUSED
Size 1

All cache banks are Paused

READS1
Size 10

Number of items of read data SLC bank 1 has in internal pipeline FIFO's

READS0
Size 10

Number of items of read data SLC bank 0 has in internal pipeline FIFO's

READS1_EXT
Size 8

Number of items of read data SLC bank 1 has outstanding from external memory

READS0_EXT
Size 8

Number of items of read data SLC bank 0 has outstanding from external memory

ROGUE_CR_SLC_STATUS2
Size: 64

Address: 0x0000e218**Default:** N/A

Type: Register**Direction**: read-only**GENERATE_POL:** NO**SCOPE:** DEBUG

Register banks: slc_dv slc

Kick pipeline: global

63	62	61	60	59	58	57	56
SLC_SIZE_IN_KB (_) ...							

55	54	53	52	51	50	49	48
SLC_SIZE_IN_KB (_)							

47	46	45	44	43	42	41	40
BUS3_OUTSTANDING_WRITES (_) ...							

39	38	37	36	35	34	33	32
BUS3_OUTSTANDING_WRITES (_)				BUS2_OUTSTANDING_WRITES (_) ...			

31	30	29	28	27	26	25	24
BUS2_OUTSTANDING_WRITES (_)							

23	22	21	20	19	18	17	16
BUS3_OUTSTANDING_READS (_) ...							

15	14	13	12	11	10	9	8
BUS3_OUTSTANDING_READS (_)				BUS2_OUTSTANDING_READS (_) ...			

7	6	5	4	3	2	1	0
BUS2_OUTSTANDING_READS (_) ...							

Current status of the SLC external interfaces and ACE Converters

Name	MSB	LSB	Default	Description	Bank Filter
SLC_SIZE_IN_KB	63	48	---	The size of the SLC in KB ie 0x0400 = 1024KB = 1MB	
BUS3_OUTSTANDING_WRITES	47	36	---	Number of write Bursts ACE Converter 3 has outstanding from external memory	
BUS2_OUTSTANDING_WRITES	35	24	---	Number of write Bursts ACE Converter 2 has outstanding from external memory	
BUS3_OUTSTANDING_READS	23	12	---	Number of Words of read data ACE Converter 3 has outstanding from external memory	
BUS2_OUTSTANDING_READS	11	0	---	Number of Words of read data ACE Converter 2 has outstanding from external memory	

ROGUE_CR_SLC_STATUS2.SLC_SIZE_IN_KB

Size: 16

Type: Define

The size of the SLC in KB ie 0x0400 = 1024KB = 1MB

ROGUE_CR_SLC_STATUS2.BUS3_OUTSTANDING_WRITES

Size: 12

Type: Define

Number of write Bursts ACE Converter 3 has outstanding from external memory

ROGUE_CR_SLC_STATUS2.BUS2_OUTSTANDING_WRITES

Size: 12

Type: Define

Number of write Bursts ACE Converter 2 has outstanding from external memory

ROGUE_CR_SLC_STATUS2.BUS3_OUTSTANDING_READS

Size: 12

Type: Define

Number of Words of read data ACE Converter 3 has outstanding from external memory

ROGUE_CR_SLC_STATUS2.BUS2_OUTSTANDING_READS

Size: 12

Type: Define

Number of Words of read data ACE Converter 2 has outstanding from external memory

---

ROGUE_CR_SOFT_RESET

Size 64

Address: 0x00000100

Access: read-write

Member of groups: rascal jones tiling texas3 texas tornado slc3 slc2 slc tpu tpu_mcu_l0 pbe usc bifpmcache blackpearl ta rasterisation hub sidekick2 sidekick mars

63	62	61	60	59	58	57	56
reserved				TILING_CORE (_)	TE3 (_)	VCE (_)	VBS (_)

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
reserved					MMU (_)	*reserved*	CPU (_)

31	30	29	28	27	26	25	24
RASCAL_CORE (_)	DUST_B_CORE (_)	DUST_A_CORE (_)	*reserved*	SLC (_)	*reserved*	UVS (_)	TE (_)

23	22	21	20	19	18	17	16
GPP (_)	*reserved*		PM (_)	PBE (_)	USC_SHARED (_)	MCU_L1 (_)	BIF (_)

15	14	13	12	11	10	9	8
CDM (_)	VDM (_)	*reserved*	PDS (_)	ISP (_)	TSP (_)	*reserved*	

7	6	5	4	3	2	1	0
reserved		SYSARB (_)	TPU_MCU_DEMUX (_)	MCU_L0 (_)	TPU (_)	*reserved*	USC (_) ...

Core soft reset control register. Write a '1' to reset and a '0' to clear See the soft reset section in the TRM to understand how to use the soft reset register.

Name	Type	MSB	LSB	Default
TILING_CORE	_	59	59	---
TE3	_	58	58	---
VCE	_	57	57	---
VBS	_	56	56	---
MMU	_	34	34	---
CPU	_	32	32	---
RASCAL_CORE	_	31	31	---
DUST_B_CORE	_	30	30	---
DUST_A_CORE	_	29	29	---
SLC	_	27	27	---
UVS	_	25	25	---

TE	_	24	24	---
GPP	_	23	23	---
PM	_	20	20	---
PBE	_	19	19	---
USC_SHARED	_	18	18	---
MCU_L1	_	17	17	---
BIF	_	16	16	---
CDM	_	15	15	---
VDM	_	14	14	---
PDS	_	12	12	---
ISP	_	11	11	---
TSP	_	10	10	---
SYSARB	_	5	5	---
TPU_MCU_DEMUX	_	4	4	---
MCU_L0	_	3	3	---
TPU	_	2	2	---
USC	_	0	0	---

USC
Size 1

TPU
Size 1

MCU_L0
Size 1

TPU_MCU_DEMUX
Size 1

SYSARB
Size 1

TSP
Size 1

ISP
Size 1

PDS
Size 1

VDM
Size 1

CDM
Size 1

BIF
Size 1

Bifpmcache BIF

MCU_L1
Size 1

USC_SHARED
Size 1

PBE
Size 1

PM
Size 1

GPP
Size 1

TE
Size 1

UVS
Size 1

SLC
Size 1

DUST_A_CORE
Size 1

DUST_B_CORE
Size 1

RASCAL_CORE
Size 1

Note that the RASL_CORE bit affects logic related to the reading and writing of registers. This soft reset should therefore be used with caution. Upon power down events it is necessary to reset every register, so this bit should be used, but it must be release before any other resets, or beofre anyu other registers are programmed

CPU
Size 1

Includes MTS and META or MIPS

MMU
Size 1

VBS
Size 1

VCE
Size 1

TE3
Size 1

TILING_CORE
Size 1

ROGUE_CR_SOFT_RESET2
Size 32

Address: 0x00000108

Access: read-write

Member of groups: hub slc3 tpu usc blackpearl jones

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved							

15	14	13	12	11	10	9	8
reserved					ASTC (_)	BLACKPEARL (_)	*reserved*

7	6	5	4	3	2	1	0
IPF (_)	GEOMETRY (_)	USC_SHARED (_)	PDS_SHARED (_)	BIF_BLACKPEARL (_)	PIXEL (_)	*reserved*	VERTEX (_) ...

Core soft reset control register. Write a '1' to reset and a '0' to clear See the soft reset section in the TRM to understand how to use the soft reset register.

Name	Type	MSB	LSB	Default
ASTC	_	10	10	---
BLACKPEARL	_	9	9	---
IPF	_	7	7	---
GEOMETRY	_	6	6	---
USC_SHARED	_	5	5	---
PDS_SHARED	_	4	4	---
BIF_BLACKPEARL	_	3	3	---
PIXEL	_	2	2	---
VERTEX	_	0	0	---

VERTEX
Size 1

PIXEL
Size 1

BIF_BLACKPEARL
Size 1

PDS_SHARED
Size 1

USC_SHARED
Size 1

GEOMETRY
Size 1

IPF
Size 1

BLACKPEARL
Size 1

ASTC
Size 1

ROGUE_CR_SYS_BUS_SECURE
Size 1

Address: 0x0000a100

Access: read-write

Member of groups: jones mars

7	6	5	4	3	2	1	0
-							Enable (_) ...

Setting this register secures the IMG Configuration Registers from the System Bus. In secure mode all registers have read access only by default. When secure mode is being set, the register must be read back to confirm that the value has propagated throug the pipeline.

Name	Type	MSB	LSB	Default
Enable	_	0	0	0x1

Enable
Size 1

0 = No System Bus Security

1 = System Bus Restricted

ROGUE_CR_TA_PERF
Size 5

Address: 0x00007600

Access: read-write

Member of groups: tiling_perf ta_perf

7	6	5	4	3	2	1	0
-			CLR_3 (_)	CLR_2 (_)	CLR_1 (_)	CLR_0 (_)	CTRL_ENABLE (_) ...

Name	Type	MSB	LSB	Default
CLR_3	_	4	4	0
CLR_2	_	3	3	0
CLR_1	_	2	2	0
CLR_0	_	1	1	0
CTRL_ENABLE	_	0	0	0

CLR_3
Size 1

clear counter 3

CLR_2
Size 1

clear counter 2

CLR_1
Size 1

clear counter 1

CLR_0
Size 1

clear counter 0

CTRL_ENABLE
Size 1

enables the perf bus counters

ROGUE_CR_TA_PERF_COUNTER_0
Size 32

Address: 0x00007650

Access: readonly

Member of groups: tiling_perf ta_perf

31	30	29	28	27	26	25	24
REG (_) ...							

23	22	21	20	19	18	17	16
REG (_) ...							

15	14	13	12	11	10	9	8
REG (_) ...							

7	6	5	4	3	2	1	0
REG (_) ...							

Name	Type	MSB	LSB	Default
REG	_	31	0	0

REG
Size 32

counter a0

ROGUE_CR_TA_PERF_SELECT0
Size 64

Address: 0x00007608

Access: read-write

Member of groups: tiling_perf ta_perf

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
reserved							

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved		MODE (_)	GROUP_SELECT (_)				

15	14	13	12	11	10	9	8
BIT_SELECT (_) ...							

7	6	5	4	3	2	1	0
BIT_SELECT (_) ...							

Name	Type	MSB	LSB	Default
MODE	_	21	21	0
GROUP_SELECT	_	20	16	0
BIT_SELECT	_	15	0	0

MODE
Size 1

reduction mode, 0: bitwise increments, 1: unsigned count increment

GROUP_SELECT
Size 5

group select, see full PERF documentation for signals in each group

BIT_SELECT
Size 16

bit mask for enabled signals in group

ROGUE_CR_TEXAS3_PERF_INDIRECT
Size 3

Address: 0x000083d0

Access: read-write

Member of groups: texas3_perf

7	6	5	4	3	2	1	0
-					ADDRESS (_) ...		

Name	MSB	LSB	Default
ADDRESS	2	0	---

ROGUE_CR_TEXAS_BIF_FAULT_BANK0_MMU_STATUS
Size 16

Address: 0x00001430

Access: readonly

Member of groups: texas3 texas

15	14	13	12	11	10	9	8
CAT_BASE (_)				*reserved*	PAGE_SIZE (_)		

7	6	5	4	3	2	1	0
reserved	DATA_TYPE (_)		FAULT_RO (_)	*reserved*	FAULT_PM_META_RO (_)	*reserved*	FAULT (_) ...

Indicates a fault has occurred on bank 0 and provides details of fault

Name	Type	MSB	LSB	Default
CAT_BASE	_	15	12	0
PAGE_SIZE	_	10	8	0
DATA_TYPE	_	6	5	0
FAULT_RO	_	4	4	0
FAULT_PM_META_RO	_	2	2	0
FAULT	_	0	0	0

CAT_BASE
Size 4

Catalogue base address number

PAGE_SIZE
Size 3

Page size

DATA_TYPE
Size 2

MMU data type that was invalid (on valid fault)

FAULT_RO
Size 1

Indicates read-only fault('1') or valid fault('0')

FAULT_PM_META_RO
Size 1

Indicates pm/meta protected region fault

FAULT
Size 1

Indicates a fault has occured

ROGUE_CR_TEXAS_BIF_FAULT_BANK0_REQ_STATUS
Size 51

Address: 0x00001438

Access: readonly

Member of groups: texas3 texas

55	54	53	52	51	50	49	48
-					RNW (_)	TAG_SB (_) ...	

47	46	45	44	43	42	41	40
TAG_SB (_)				TAG_ID (_)			

39	38	37	36	35	34	33	32
ADDRESS (_) ...							

31	30	29	28	27	26	25	24
ADDRESS (_) ...							

23	22	21	20	19	18	17	16
ADDRESS (_) ...							

15	14	13	12	11	10	9	8
ADDRESS (_) ...							

7	6	5	4	3	2	1	0
ADDRESS (_)				*reserved*			

Provides details of the request that faulted on bank 0

Name	Type	MSB	LSB	Default
RNW	_	50	50	0
TAG_SB	_	49	44	0
TAG_ID	_	43	40	0
ADDRESS	_	39	4	0

RNW
Size 1

TAG_SB
Size 6

TAG_ID
Size 4

ADDRESS
Size 36

ROGUE_CR_TEXAS_PERF
Size 7

Address: 0x00008290

Access: read-write

Member of groups: texas3_perf texas_perf

7	6	5	4	3	2	1	0
-	CLR_5 (_)	CLR_4 (_)	CLR_3 (_)	CLR_2 (_)	CLR_1 (_)	CLR_0 (_)	CTRL_ENABLE (_) ...

Name	MSB	LSB	Default
CLR_5	6	6	0
CLR_4	5	5	0
CLR_3	4	4	0
CLR_2	3	3	0
CLR_1	2	2	0
CLR_0	1	1	0
CTRL_ENABLE	0	0	0

CLR_5
Size 1

clear counter 3

CLR_4
Size 1

clear counter 3

CLR_3
Size 1

clear counter 3

CLR_2
Size 1

clear counter 2

CLR_1
Size 1

clear counter 1

CLR_0
Size 1

clear counter 0

CTRL_ENABLE
Size 1

enables the perf bus counters

ROGUE_CR_TEXAS_PERF_COUNTER_0
Size 32

Address: 0x000082d8

Access: readonly

Member of groups: texas3_perf texas_perf

31	30	29	28	27	26	25	24
REG (_) ...							

23	22	21	20	19	18	17	16
REG (_) ...							

15	14	13	12	11	10	9	8
REG (_) ...							

7	6	5	4	3	2	1	0
REG (_) ...							

Name	MSB	LSB	Default
REG	31	0	0

REG
Size 32

counter a0

ROGUE_CR_TEXAS_PERF_INDIRECT
Size 2

Address: 0x00008288

Access: read-write

Member of groups: texas_perf

7	6	5	4	3	2	1	0
-						ADDRESS (_) ...	

Name	MSB	LSB	Default

ADDRESS	1	0	---

ROGUE_CR_TEXAS_PERF_SELECT0

Size 64

Address: 0x00008298

Access: read-write

Member of groups: texas3_perf texas_perf

63	62	61	60	59	58	57	56
reserved						BATCH_MAX (_) ...	

55	54	53	52	51	50	49	48
BATCH_MAX (_)							

47	46	45	44	43	42	41	40
reserved						BATCH_MIN (_) ...	

39	38	37	36	35	34	33	32
BATCH_MIN (_)							

31	30	29	28	27	26	25	24
MODE (_)	*reserved*						

23	22	21	20	19	18	17	16
reserved					GROUP_SELECT (_)		

15	14	13	12	11	10	9	8
BIT_SELECT (_) ...							

7	6	5	4	3	2	1	0
BIT_SELECT (_) ...							

Name	MSB	LSB	Default
BATCH_MAX	61	48	0x3fff
BATCH_MIN	45	32	0
MODE	31	31	0
GROUP_SELECT	21	16	0
BIT_SELECT	15	0	0

BATCH_MAX

Size 14

this is the max batch number which will be counted in this group

BATCH_MIN

Size 14

this is the min batch number which will be counted in this group

MODE

Size 1

reduction mode, 0: bitwise increments, 1: unsigned count increment

GROUP_SELECT
Size 6

group select, see full PERF documentation for signals in each group

BIT_SELECT
Size 16

bit mask for enabled signals in group

ROGUE_CR_TIMER
Size 64

Address: 0x00000160

Access: readonly

Member of groups: jones mars

63	62	61	60	59	58	57	56
BIT31 (_)	*reserved*						

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
VALUE (_) ...							

39	38	37	36	35	34	33	32
VALUE (_) ...							

31	30	29	28	27	26	25	24
VALUE (_) ...							

23	22	21	20	19	18	17	16
VALUE (_) ...							

15	14	13	12	11	10	9	8
VALUE (_) ...							

7	6	5	4	3	2	1	0
VALUE (_) ...							

This register contains the value of a 48-bit internal timer. The timer runs continuously, and wraps at the top end. It counts 256 cycles at the core clock frequency. This means that at 100 MHz: 1 count value = 1/100MHz = 256 * 10 * 10^-9 seconds = 2.56 us In order to avoid having to issue three 32-bit reads to detect the lower 32-bits wrapping, the MSB of the low 32-bit word is duplicated in the MSB of the high 32-bit word.

Name	Type	MSB	LSB	Default
BIT31	_	63	63	---
VALUE	_	47	0	---

BIT31
Size 1

VALUE
Size 48

ROGUE_CR_TORNADO_PERF
Size 5

Address: 0x00008228

Access: read-write

Member of groups: tornado_perf

7	6	5	4	3	2	1	0
-			CLR_3 (_)	CLR_2 (_)	CLR_1 (_)	CLR_0 (_)	CTRL_ENABLE (_) ...

Name	MSB	LSB	Default
CLR_3	4	4	0
CLR_2	3	3	0
CLR_1	2	2	0
CLR_0	1	1	0
CTRL_ENABLE	0	0	0

CLR_3
Size 1

clear counter 3

CLR_2
Size 1

clear counter 2

CLR_1
Size 1

clear counter 1

CLR_0
Size 1

clear counter 0

CTRL_ENABLE
Size 1

enables the perf bus counters

ROGUE_CR_TORNADO_PERF_COUNTER_0
Size 32

Address: 0x00008268

Access: readonly

Member of groups: tornado_perf

31	30	29	28	27	26	25	24
REG (_) ...							

23	22	21	20	19	18	17	16
REG (_) ...							

15	14	13	12	11	10	9	8
REG (_) ...							

7	6	5	4	3	2	1	0
REG (_) ...							

Name	MSB	LSB	Default
REG	31	0	0

REG

Size 32

counter a0

ROGUE_CR_TORNADO_PERF_SELECT0

Size 64

Address: 0x00008230

Access: read-write

Member of groups: tornado_perf

63	62	61	60	59	58	57	56
reserved		BATCH_MAX (_) ...					

55	54	53	52	51	50	49	48
BATCH_MAX (_)							

47	46	45	44	43	42	41	40
reserved		BATCH_MIN (_) ...					

39	38	37	36	35	34	33	32
BATCH_MIN (_)							

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved		MODE (_)	GROUP_SELECT (_)				

15	14	13	12	11	10	9	8
BIT_SELECT (_) ...							

7	6	5	4	3	2	1	0
BIT_SELECT (_) ...							

Name	MSB	LSB	Default
BATCH_MAX	61	48	0x3fff
BATCH_MIN	45	32	0
MODE	21	21	0

GROUP_SELECT	20	16	0
BIT_SELECT	15	0	0

BATCH_MAX
Size 14

this is the max batch number which will be counted in this group

BATCH_MIN
Size 14

this is the min batch number which will be counted in this group

MODE
Size 1

reduction mode, 0: bitwise increments, 1: unsigned count increment

GROUP_SELECT
Size 5

group select, see full PERF documentation for signals in each group

BIT_SELECT
Size 16

bit mask for enabled signals in group

ROGUE_CR_TPU_MCU_L0_PERF
Size 5

Address: 0x00007900

Access: read-write

Member of groups: tpu_perf tpu_mcu_l0_perf

7	6	5	4	3	2	1	0
-			CLR_3 (_)	CLR_2 (_)	CLR_1 (_)	CLR_0 (_)	CTRL_ENABLE (_) ...

Name	Type	MSB	LSB	Default
CLR_3	_	4	4	0
CLR_2	_	3	3	0
CLR_1	_	2	2	0
CLR_0	_	1	1	0
CTRL_ENABLE	_	0	0	0

CLR_3
Size 1

clear counter 3

CLR_2
Size 1

clear counter 2

CLR_1
Size 1

clear counter 1

CLR_0
Size 1

clear counter 0

CTRL_ENABLE
Size 1

enables the perf bus counters

ROGUE_CR_TPU_MCU_L0_PERF_COUNTER_0
Size 32

Address: 0x00007950

Access: readonly

Member of groups: tpu_perf tpu_mcu_l0_perf

31	30	29	28	27	26	25	24
REG (_) ...							

23	22	21	20	19	18	17	16
REG (_) ...							

15	14	13	12	11	10	9	8
REG (_) ...							

7	6	5	4	3	2	1	0
REG (_) ...							

Name	Type	MSB	LSB	Default
REG	_	31	0	0

REG
Size 32

counter a0

ROGUE_CR_TPU_MCU_L0_PERF_INDIRECT
Size 3

Address: 0x00008028

Access: read-write

Member of groups: tpu_mcu_l0_perf

7	6	5	4	3	2	1	0
-					ADDRESS (_) ...		

Name	MSB	LSB	Default

ADDRESS	2	0	---

ROGUE_CR_TPU_MCU_L0_PERF_SELECT0

Size 64

Address: 0x00007908

Access: read-write

Member of groups: tpu_perf tpu_mcu_l0_perf

63	62	61	60	59	58	57	56
reserved		BATCH_MAX (_) ...					

55	54	53	52	51	50	49	48
BATCH_MAX (_)							

47	46	45	44	43	42	41	40
reserved		BATCH_MIN (_) ...					

39	38	37	36	35	34	33	32
BATCH_MIN (_)							

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved		MODE (_)	GROUP_SELECT (_)				

15	14	13	12	11	10	9	8
BIT_SELECT (_) ...							

7	6	5	4	3	2	1	0
BIT_SELECT (_) ...							

Name	Type	MSB	LSB	Default
BATCH_MAX	_	61	48	0x3fff
BATCH_MIN	_	45	32	0
MODE	_	21	21	0
GROUP_SELECT	_	20	16	0
BIT_SELECT	_	15	0	0

BATCH_MAX

Size 14

this is the min batch number which will be counted in this group

BATCH_MIN

Size 14

this is the min batch number which will be counted in this group

MODE

Size 1

reduction mode, 0: bitwise increments, 1: unsigned count increment

GROUP_SELECT
Size 5

group select, see full PERF documentation for signals in each group

BIT_SELECT
Size 16

bit mask for enabled signals in group

ROGUE_CR_TPU_PERF_INDIRECT
Size 3

Address: 0x000083f0

Access: read-write

Member of groups: tpu_perf

7	6	5	4	3	2	1	0
-					ADDRESS (_) ...		

Name	MSB	LSB	Default
ADDRESS	2	0	---

ROGUE_CR_USC_PERF
Size 5

Address: 0x00008100

Access: read-write

Member of groups: usc_perf

7	6	5	4	3	2	1	0
-			CLR_3 (_)	CLR_2 (_)	CLR_1 (_)	CLR_0 (_)	CTRL_ENABLE (_) ...

Name	Type	MSB	LSB	Default
CLR_3	_	4	4	0
CLR_2	_	3	3	0
CLR_1	_	2	2	0
CLR_0	_	1	1	0
CTRL_ENABLE	_	0	0	0

CLR_3
Size 1

clear counter 3

CLR_2
Size 1

clear counter 2

CLR_1
Size 1

clear counter 1

CLR_0
Size 1

clear counter 0

CTRL_ENABLE
Size 1

enables the perf bus counters

ROGUE_CR_USC_PERF_COUNTER_0
Size 32

Address: 0x00008150

Access: readonly

Member of groups: usc_perf

31	30	29	28	27	26	25	24
REG (_) ...							

23	22	21	20	19	18	17	16
REG (_) ...							

15	14	13	12	11	10	9	8
REG (_) ...							

7	6	5	4	3	2	1	0
REG (_) ...							

Name	Type	MSB	LSB	Default
REG	_	31	0	0

REG
Size 32

counter a0

ROGUE_CR_USC_PERF_INDIRECT
Size 4

Address: 0x00008030

Access: read-write

Member of groups: usc_perf

7	6	5	4	3	2	1	0
-				ADDRESS (_) ...			

Name	MSB	LSB	Default
ADDRESS	3	0	---

ROGUE_CR_USC_PERF_SELECT0

Size 64

Address: 0x00008108

Access: read-write

Member of groups: usc_perf

63	62	61	60	59	58	57	56
reserved		BATCH_MAX (_) ...					

55	54	53	52	51	50	49	48
BATCH_MAX (_)							

47	46	45	44	43	42	41	40
reserved		BATCH_MIN (_) ...					

39	38	37	36	35	34	33	32
BATCH_MIN (_)							

31	30	29	28	27	26	25	24
reserved							

23	22	21	20	19	18	17	16
reserved		MODE (_)	GROUP_SELECT (_)				

15	14	13	12	11	10	9	8
BIT_SELECT (_) ...							

7	6	5	4	3	2	1	0
BIT_SELECT (_) ...							

Name	Type	MSB	LSB	Default
BATCH_MAX	_	61	48	0x3fff
BATCH_MIN	_	45	32	0
MODE	_	21	21	0
GROUP_SELECT	_	20	16	0
BIT_SELECT	_	15	0	0

BATCH_MAX

Size 14

this is the min batch number which will be counted in this group

BATCH_MIN

Size 14

this is the min batch number which will be counted in this group

MODE

Size 1

reduction mode, 0: bitwise increments, 1: unsigned count increment

GROUP_SELECT
Size 5

group select, see full PERF documentation usc for signals in each group

BIT_SELECT
Size 16

bit mask for enabled signals in group

ROGUE_CR_VDM_CONTEXT_STORE_MODE
Size 2

Address: 0x0000f048

Access: read-write

Member of groups: jones

7	6	5	4	3	2	1	0
-						MODE (_) ... = *INDEX*	

This register defines the TA context switching granularity. INDEX is the fastest; LIST is the slowest. This register must be programmed before writing to ROGUE_CR_VDM_CONTEXT_STORE_START_PULSE.

Name	MSB	LSB	Default
MODE	1	0	INDEX [0]

MODE
Size 2

Possible Values:

Name	Value/Range	Info
INDEX	0 [0]	Stop at the end of the index
INSTANCE	1 [0x1]	Stop at the end of the instance
LIST	2 [0x2]	Stop at the end of the list

ROGUE_CR_MIPS_ADDR_REMAP1_CONFIG1
Size 48

Address: 0x00000818

Access: read-write

Member of groups: sidekick2 sidekick

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
reserved							

31	30	29	28	27	26	25	24
BASE_ADDR_IN (_) ...							

23	22	21	20	19	18	17	16
BASE_ADDR_IN (_) ...							

15	14	13	12	11	10	9	8
BASE_ADDR_IN (_)				*reserved*			

7	6	5	4	3	2	1	0
reserved							MODE_ENABLE (_) ...

This register contains the address remapping options for the MIPS CPU physical address, e.g. during boot

Name	Type	MSB	LSB	Default
BASE_ADDR_IN	_	31	12	0x1fc00
MODE_ENABLE	_	0	0	0

MODE_ENABLE

Size 1

Enable address remapping mode

BASE_ADDR_IN

Size 20

4K (12 bits) aligned address used as a input for the address remapping

ROGUE_CR_MIPS_ADDR_REMAP1_CONFIG2

Size 48

Address: 0x00000820

Access: read-write

Member of groups: sidekick2 sidekick

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
ADDR_OUT (_) ...							

31	30	29	28	27	26	25	24
ADDR_OUT (_) ...							

23	22	21	20	19	18	17	16
ADDR_OUT (_) ...							

15	14	13	12	11	10	9	8
ADDR_OUT (_)				*reserved*			OS_ID (_) ...

7	6	5	4	3	2	1	0
OS_ID (_)		TRUSTED (_)		REGION_SIZE_POW2 (_) ...			

This register contains the address remapping options for the MIPS CPU physical address, e.g. during boot

Name	Type	MSB	LSB	Default
ADDR_OUT	_	39	12	0
OS_ID	_	8	6	0
TRUSTED	_	5	5	0
REGION_SIZE_POW2	_	4	0	0xc

REGION_SIZE_POW2
Size 5

Remapped region size or offset size, i.e. number of bits from the bottom of the base input address that survive onto the output address. Minimum value of 12

TRUSTED
Size 1

Defines whether these accesses are trusted

OS_ID
Size 3

The OS_ID emitted for all address transactions from this region

ADDR_OUT
Size 28

4K (12 bits) aligned address used as output for the address remapping

---

ROGUE_CR_MIPS_ADDR_REMAP2_CONFIG1
Size 48

Address: 0x00000828

Access: read-write

Member of groups: sidekick2 sidekick

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
reserved							

31	30	29	28	27	26	25	24
BASE_ADDR_IN (_) ...							

23	22	21	20	19	18	17	16
BASE_ADDR_IN (_) ...							

15	14	13	12	11	10	9	8
BASE_ADDR_IN (_)				*reserved*			

7	6	5	4	3	2	1	0
reserved							MODE_ENABLE (_) ...

This register contains the address remapping options for the MIPS CPU physical address, e.g. during boot

Name	Type	MSB	LSB	Default
BASE_ADDR_IN	_	31	12	0x1fc00
MODE_ENABLE	_	0	0	0

MODE_ENABLE
Size 1

Enable address remapping mode

BASE_ADDR_IN
Size 20

4K (12 bits) aligned address used as a input for the address remapping

---

ROGUE_CR_MIPS_ADDR_REMAP2_CONFIG2
Size 48

Address: 0x00000830

Access: read-write

Member of groups: sidekick2 sidekick

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
ADDR_OUT (_) ...							

31	30	29	28	27	26	25	24
ADDR_OUT (_) ...							

23	22	21	20	19	18	17	16
ADDR_OUT (_) ...							

15	14	13	12	11	10	9	8
ADDR_OUT (_)				*reserved*			OS_ID (_) ...

7	6	5	4	3	2	1	0
OS_ID (_)		TRUSTED (_)	REGION_SIZE_POW2 (_) ...				

This register contains the address remapping options for the MIPS CPU physical address, e.g. during boot

Name	Type	MSB	LSB	Default
ADDR_OUT	_	39	12	0
OS_ID	_	8	6	0
TRUSTED	_	5	5	0
REGION_SIZE_POW2	_	4	0	0xc

REGION_SIZE_POW2
Size 5

Remapped region size or offset size, i.e. number of bits from the bottom of the base input address that survive onto the output address. Minimum value of 12

TRUSTED
Size 1

Defines whether these accesses are trusted

OS_ID
Size 3

The OS_ID emitted for all address transactions from this region

ADDR_OUT

Size 28

4K (12 bits) aligned address used as output for the address remapping

ROGUE_CR_MIPS_ADDR_REMAP3_CONFIG1

Size 48

Address: 0x00000838

Access: read-write

Member of groups: sidekick2 sidekick

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
reserved							

31	30	29	28	27	26	25	24
BASE_ADDR_IN (_) ...							

23	22	21	20	19	18	17	16
BASE_ADDR_IN (_) ...							

15	14	13	12	11	10	9	8
BASE_ADDR_IN (_)				*reserved*			

7	6	5	4	3	2	1	0
reserved							MODE_ENABLE (_) ...

This register contains the address remapping options for the MIPS CPU physical address, e.g. during boot

Name	Type	MSB	LSB	Default
BASE_ADDR_IN	_	31	12	0x1fc00
MODE_ENABLE	_	0	0	0

MODE_ENABLE

Size 1

Enable address remapping mode

BASE_ADDR_IN

Size 20

4K (12 bits) aligned address used as a input for the address remapping

ROGUE_CR_MIPS_ADDR_REMAP3_CONFIG2

Size 48

Address: 0x00000840

Access: read-write

Member of groups: sidekick2 sidekick

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
ADDR_OUT (_) ...							

31	30	29	28	27	26	25	24
ADDR_OUT (_) ...							

23	22	21	20	19	18	17	16
ADDR_OUT (_) ...							

15	14	13	12	11	10	9	8
ADDR_OUT (_)				*reserved*			OS_ID (_) ...

7	6	5	4	3	2	1	0
OS_ID (_)		TRUSTED (_)	REGION_SIZE_POW2 (_) ...				

This register contains the address remapping options for the MIPS CPU physical address, e.g. during boot

Name	Type	MSB	LSB	Default
ADDR_OUT	_	39	12	0
OS_ID	_	8	6	0
TRUSTED	_	5	5	0
REGION_SIZE_POW2	_	4	0	0xc

REGION_SIZE_POW2

Size 5

Remapped region size or offset size, i.e. number of bits from the bottom of the base input address that survive onto the output address. Minimum value of 12

TRUSTED

Size 1

Defines whether these accesses are trusted

OS_ID

Size 3

The OS_ID emitted for all address transactions from this region

ADDR_OUT

Size 28

4K (12 bits) aligned address used as output for the address remapping

ROGUE_CR_MIPS_ADDR_REMAP4_CONFIG1

Size 48

Address: 0x00000848

Access: read-write

Member of groups: sidekick2 sidekick

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32

reserved

31	30	29	28	27	26	25	24
BASE_ADDR_IN (_) ...							

23	22	21	20	19	18	17	16
BASE_ADDR_IN (_) ...							

15	14	13	12	11	10	9	8
BASE_ADDR_IN (_)				*reserved*			

7	6	5	4	3	2	1	0
reserved							MODE_ENABLE (_) ...

This register contains the address remapping options for the MIPS CPU physical address, e.g. during boot

Name	Type	MSB	LSB	Default
BASE_ADDR_IN	_	31	12	0x1fc00
MODE_ENABLE	_	0	0	0

MODE_ENABLE

Size 1

Enable address remapping mode

BASE_ADDR_IN

Size 20

4K (12 bits) aligned address used as a input for the address remapping

ROGUE_CR_MIPS_ADDR_REMAP4_CONFIG2

Size 48

Address: 0x00000850

Access: read-write

Member of groups: sidekick2 sidekick

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
ADDR_OUT (_) ...							

31	30	29	28	27	26	25	24
ADDR_OUT (_) ...							

23	22	21	20	19	18	17	16
ADDR_OUT (_) ...							

15	14	13	12	11	10	9	8
ADDR_OUT (_)				*reserved*			OS_ID (_) ...

7	6	5	4	3	2	1	0
OS_ID (_)		TRUSTED (_)		REGION_SIZE_POW2 (_) ...			

This register contains the address remapping options for the MIPS CPU physical address, e.g. during boot

Name	Type	MSB	LSB	Default
ADDR_OUT	_	39	12	0
OS_ID	_	8	6	0
TRUSTED	_	5	5	0
REGION_SIZE_POW2	_	4	0	0xc

REGION_SIZE_POW2
Size 5

Remapped region size or offset size, i.e. number of bits from the bottom of the base input address that survive onto the output address. Minimum value of 12

TRUSTED
Size 1

Defines whether these accesses are trusted

OS_ID
Size 3

The OS_ID emitted for all address transactions from this region

ADDR_OUT
Size 28

4K (12 bits) aligned address used as output for the address remapping

---

ROGUE_CR_MIPS_ADDR_REMAP5_CONFIG1
Size 48

Address: 0x00000858

Access: read-write

Member of groups: sidekick2 sidekick

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
reserved							

31	30	29	28	27	26	25	24
BASE_ADDR_IN (_) ...							

23	22	21	20	19	18	17	16
BASE_ADDR_IN (_) ...							

15	14	13	12	11	10	9	8
BASE_ADDR_IN (_)				*reserved*			

7	6	5	4	3	2	1	0
reserved							MODE_ENABLE (_) ...

This register contains the address remapping options for the MIPS CPU physical address, e.g. during boot

Name	Type	MSB	LSB	Default

BASE_ADDR_IN	_	31	12	0x1fc00
MODE_ENABLE	_	0	0	0

MODE_ENABLE
Size 1

Enable address remapping mode

BASE_ADDR_IN
Size 20

4K (12 bits) aligned address used as a input for the address remapping

ROGUE_CR_MIPS_ADDR_REMAP5_CONFIG2
Size 48

Address: 0x00000860

Access: read-write

Member of groups: sidekick2 sidekick

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
ADDR_OUT (_) ...							

31	30	29	28	27	26	25	24
ADDR_OUT (_) ...							

23	22	21	20	19	18	17	16
ADDR_OUT (_) ...							

15	14	13	12	11	10	9	8
ADDR_OUT (_)				*reserved*			OS_ID (_) ...

7	6	5	4	3	2	1	0
OS_ID (_)		TRUSTED (_)		REGION_SIZE_POW2 (_) ...			

This register contains the address remapping options for the MIPS CPU physical address, e.g. during boot

Name	Type	MSB	LSB	Default
ADDR_OUT	_	39	12	0
OS_ID	_	8	6	0
TRUSTED	_	5	5	0
REGION_SIZE_POW2	_	4	0	0xc

REGION_SIZE_POW2
Size 5

Remapped region size or offset size, i.e. number of bits from the bottom of the base input address that survive onto the output address. Minimum value of 12

TRUSTED
Size 1

Defines whether these accesses are trusted

OS_ID
Size 3

The OS_ID emitted for all address transactions from this region

ADDR_OUT
Size 28

4K (12 bits) aligned address used as output for the address remapping

ROGUE_CR_MIPS_DEBUG_CONFIG
Size 1

Address: 0x000008c8

Access: read-write

Member of groups: sidekick2 sidekick

7	6	5	4	3	2	1	0
-							DISABLE_PROBE_DEBUG (_) ...

This register contains the security and debug configuration options for the MIPS GPU scheduler.

Name	Type	MSB	LSB	Default
DISABLE_PROBE_DEBUG	_	0	0	0x1

DISABLE_PROBE_DEBUG
Size 1

Enable MIPS SecureDebug. Disables EJTAG access to the MIPS core and PC Sampling

ROGUE_CR_MIPS_EXCEPTION_STATUS
Size 6

Address: 0x000008d0

Access: readonly

Member of groups: sidekick2 sidekick

7	6	5	4	3	2	1	0
-	SI_SLEEP (_)	SI_NMI_TAKEN (_)	SI_NEST_EXL (_)	SI_NEST_ERL (_)	SI_EXL (_)	SI_ERL (_) ...	

This register contains the exception status information of the MIPS GPU scheduler.

Name	Type	MSB	LSB	Default
SI_SLEEP	_	5	5	0
SI_NMI_TAKEN	_	4	4	0
SI_NEST_EXL	_	3	3	0
SI_NEST_ERL	_	2	2	0
SI_EXL	_	1	1	0
SI_ERL	_	0	0	0x1

SI_ERL
Size 1

Reflects the status of the MIPS SI_ERL pin

SI_EXL
Size 1

Reflects the status of the MIPS SI_EXL pin

SI_NEST_ERL
Size 1

Reflects the status of the MIPS SI_NESTERL pin

SI_NEST_EXL
Size 1

Reflects the status of the MIPS SI_NESTEXL pin

SI_NMI_TAKEN
Size 1

Reflects the status of the MIPS SI_NMITaken pin

SI_SLEEP
Size 1

Reflects the status of the MIPS SI_Sleep pin

ROGUE_CR_MIPS_WRAPPER_CONFIG
Size 64

Address: 0x00000810

Access: read-write

Member of groups: sidekick2 sidekick

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
reserved							FW_IDLE_ENABLE (_)

39	38	37	36	35	34	33	32
reserved						DISABLE_BOOT (_)	L2_CACHE_OFF (_)

31	30	29	28	27	26	25	24
reserved				OS_ID (_)			TRUSTED (_)

23	22	21	20	19	18	17	16
reserved							BOOT_ISA_MODE (ISA_MODES) = *MICROMIPS*

15	14	13	12	11	10	9	8
REGBANK_BASE_ADDR (_) ...							

7	6	5	4	3	2	1	0

REGBANK_BASE_ADDR (_) ...

This register contains the configuration options for the MIPS CPU wrapper.

Name	Type	MSB	LSB	Default
FW_IDLE_ENABLE	_	40	40	0
DISABLE_BOOT	_	33	33	0
L2_CACHE_OFF	_	32	32	0
OS_ID	_	27	25	0
TRUSTED	_	24	24	0
BOOT_ISA_MODE	ISA_MODES	16	16	MICROMIPS [0x1]
REGBANK_BASE_ADDR	_	15	0	0

ISA_MODES

Size 1

Boot up mode for MIPS

Possible Values:

Name	Value/Range	Info
MIPS32	0 [0]	MIPS32 ISA boot mode
MICROMIPS	1 [0x1]	MicroMIPS ISA boot mode

REGBANK_BASE_ADDR

Size 16

16-bit aligned address that identifies rgx register bank transactions emitted from the MIPS core

TRUSTED

Size 1

Defines whether these accesses are trusted

OS_ID

Size 3

The default OS_ID of the firmware

L2_CACHE_OFF

Size 1

Turn off the L2 cache within the MIPS wrapper

DISABLE_BOOT

Size 1

Stop the MIPS from boot-up even after a soft reset is triggered

FW_IDLE_ENABLE

Size 1

Set to 0x0 overwrites the value of GPU_IDLE to 0x0, set to 0x1 makes GPU Idle dependent on top level idles

EVENT

Size 1

Indicates an outstanding interrupt to HOST from RGX firmware

ROGUE_CR_MIPS_WRAPPER_IRQ_CLEAR

Size 1

Address: 0x000008b0

Access: writeonly

Member of groups: sidekick2 sidekick

7	6	5	4	3	2	1	0
-							EVENT (_) ...

This register contains the configuration options for the RGX firmware interrupts to HOST.

Name	Type	MSB	LSB	Default
EVENT	_	0	0	0

EVENT

Size 1

Clears the interrupt event to HOST from RGX firmware