Rogue Registers Referenced in the Firmware Interface

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Public

Contents

ROGUE_CR_BLACKPEARL_FIX

Size 16

Address: 0x0000f0c8

Access: read-write

Member of groups: blackpearl

15	14	13	12	11	10	9	8
DISABLE (_) ...							

7	6	5	4	3	2	1	0
DISABLE (_)							ZLS_D24S8_OGL_COMPLIANT_EN (_) ...

Name	MSB	LSB	Default
DISABLE	15	1	0
ZLS_D24S8_OGL_COMPLIANT_EN	0	0	0

DISABLE

Size 15

Used to Disable ECO Fixes

ROGUE_CR_CDM_CB

Size: 40

Address: 0x000004f0**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** GPGPU

Register banks: cdm_dv jones

Kick pipeline: compute_fe

39	38	37	36	35	34	33	32
SIZE (_) ...							

31	30	29	28	27	26	25	24
SIZE (_) ...							

23	22	21	20	19	18	17	16
SIZE (_) ...							

15	14	13	12	11	10	9	8

SIZE (_) ...							

7	6	5	4	3	2	1	0
SIZE (_)						*reserved*	

CDM Circular Buffer Size in Dwords.

Name	MSB	LSB	Default	Description	Bank Filter
SIZE	39	2	---	1TB range, 32-bit granular Compute Circular Buffer Size	

SIZE

Size: 38

Type: Define

ALIGN: 2

1TB range, 32-bit granular Compute Circular Buffer Size

ROGUE_CR_CDM_CB_BASE

Size: 40

Address: 0x000004e8**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** GPGPU

Register banks: cdm_dv jones

Kick pipeline: compute_fe

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)						*reserved*	

CDM Circular Buffer Base Address.

Name	MSB	LSB	Default	Description	Bank Filter
ADDR	39	2	---	1TB range, 32-bit aligned Compute Circular Buffer base address	

ADDR

Size: 38

Type: Define

ALIGN: 2

1TB range, 32-bit aligned Compute Circular Buffer base address.

ROGUE_CR_CDM_CB_QUEUE

Size: 40

Address: 0x000004f8**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** GPGPU

Register banks: cdm_dv jones

Kick pipeline: global

39	38	37	36	35	34	33	32
CTRL_BASE_ADDR (_) ...							

31	30	29	28	27	26	25	24
CTRL_BASE_ADDR (_) ...							

23	22	21	20	19	18	17	16
CTRL_BASE_ADDR (_) ...							

15	14	13	12	11	10	9	8
CTRL_BASE_ADDR (_) ...							

7	6	5	4	3	2	1	0
CTRL_BASE_ADDR (_)	*reserved*						

CDM Circular Buffer Queue Control Base Address.

Name	MSB	LSB	Default	Description	Bank Filter
CTRL_BASE_ADDR	39	7	---	1TB range, 1024-bit aligned Compute Circular Buffer Queue Control Data Structure base address	

CTRL_BASE_ADDR

Size: 33

Type: Define

ALIGN: 7

1TB range, 1024-bit aligned Compute Circular Buffer Queue Control Data Structure base address.

ROGUE_CR_CDM_CONTEXT_LOAD_PDS0

Size 64

Address: 0x000004d8

Access: read-write

Member of groups: texas3 tornado hub

63	62	61	60	59	58	57	56
DATA_ADDR (_) ...							

55	54	53	52	51	50	49	48
DATA_ADDR (_) ...							

47	46	45	44	43	42	41	40
DATA_ADDR (_) ...							

39	38	37	36	35	34	33	32
DATA_ADDR (_)	*reserved*						

31	30	29	28	27	26	25	24
CODE_ADDR (_) ...							

23	22	21	20	19	18	17	16
CODE_ADDR (_) ...							

15	14	13	12	11	10	9	8
CODE_ADDR (_) ...							

7	6	5	4	3	2	1	0
CODE_ADDR (_)	*reserved*						

This register contains the PDS Code and Data Addresses for the Store/Load Program. This program is sent to PDS on Context Store and Context Load.

Name	Type	MSB	LSB	Default
DATA_ADDR	_	63	36	---
CODE_ADDR	_	31	4	---

DATA_ADDR

Size 28

PDS Data Address for Store/Load Program, 128-bit aligned

CODE_ADDR

Size 28

PDS Code Address for Store/Load Program, 128-bit aligned

ROGUE_CR_CDM_CONTEXT_LOAD_PDS1

Size 30

Address: 0x000004e0

Access: read-write

Member of groups: texas3 tornado hub

31	30	29	28	27	26	25	24
-	PDS_SEQ_DEP (_)	USC_SEQ_DEP (_)	TARGET (_)	UNIFIED_SIZE (_) ...			

23	22	21	20	19	18	17	16
UNIFIED_SIZE (_)	COMMON_SHARED (_)	COMMON_SIZE (_) ...					

15	14	13	12	11	10	9	8
COMMON_SIZE (_)					TEMP_SIZE (_) ...		

7	6	5	4	3	2	1	0
TEMP_SIZE (_)	DATA_SIZE (_)						FENCE (_) ...

This register contains the PDS Task Data necessary to produce the Store/Load PDS Program Task from CDM to PDS

Name	Type	MSB	LSB	Default
PDS_SEQ_DEP	_	29	29	---
USC_SEQ_DEP	_	28	28	---
TARGET	_	27	27	---
UNIFIED_SIZE	_	26	21	---
COMMON_SHARED	_	20	20	---
COMMON_SIZE	_	19	11	---
TEMP_SIZE	_	10	7	---
DATA_SIZE	_	6	1	---

FENCE	_	0	0	---

PDS_SEQ_DEP
Size 1

PDS Sequential Dependency

USC_SEQ_DEP
Size 1

USC Sequential Dependency

TARGET
Size 1

USC Target (0=All, 1=Any)

UNIFIED_SIZE
Size 6

Unified Size

COMMON_SHARED
Size 1

PDS Common Store Allocation is Shared Registers

COMMON_SIZE
Size 9

PDS Common Size

TEMP_SIZE
Size 4

PDS Temp Size

DATA_SIZE
Size 6

PDS Data Size

FENCE
Size 1

Fence the Task in the PDS/USC - Set on Store, unset on Load

ROGUE_CR_CDM_CONTEXT_PDS0
Size 64

Address: 0x000004a8

Access: read-write

Member of groups: texas3 tornado hub

63	62	61	60	59	58	57	56
DATA_ADDR (_) ...							

55	54	53	52	51	50	49	48
DATA_ADDR (_) ...							

47	46	45	44	43	42	41	40
DATA_ADDR (_) ...							

39	38	37	36	35	34	33	32
DATA_ADDR (_)				*reserved*			

31	30	29	28	27	26	25	24
CODE_ADDR (_) ...							

23	22	21	20	19	18	17	16
CODE_ADDR (_) ...							

15	14	13	12	11	10	9	8
CODE_ADDR (_) ...							

7	6	5	4	3	2	1	0
CODE_ADDR (_)				*reserved*			

This register contains the PDS Code and Data Addresses for the Store/Load Program. This program is sent to PDS on Context Store and Context Load.

Name	Type	MSB	LSB	Default
DATA_ADDR	_	63	36	---
CODE_ADDR	_	31	4	---

DATA_ADDR

Size 28

PDS Data Address for Store/Load Program, 128-bit aligned

CODE_ADDR

Size 28

PDS Code Address for Store/Load Program, 128-bit aligned

ROGUE_CR_CDM_CONTEXT_PDS1

Size 30

Address: 0x000004b0

Access: read-write

Member of groups: texas3 tornado hub

31	30	29	28	27	26	25	24
-	PDS_SEQ_DEP (_)		USC_SEQ_DEP (_)		TARGET (_)	UNIFIED_SIZE (_) ...	

23	22	21	20	19	18	17	16
UNIFIED_SIZE (_)			COMMON_SHARED (_)		COMMON_SIZE (_) ...		

15	14	13	12	11	10	9	8
COMMON_SIZE (_)				TEMP_SIZE (_) ...			

7	6	5	4	3	2	1	0

TEMP_SIZE (_) | DATA_SIZE (_) | FENCE (_) ...

This register contains the PDS Task Data necessary to produce the Store/Load PDS Program Task from CDM to PDS

Name	Type	MSB	LSB	Default
PDS_SEQ_DEP	_	29	29	---
USC_SEQ_DEP	_	28	28	---
TARGET	_	27	27	---
UNIFIED_SIZE	_	26	21	---
COMMON_SHARED	_	20	20	---
COMMON_SIZE	_	19	11	---
TEMP_SIZE	_	10	7	---
DATA_SIZE	_	6	1	---
FENCE	_	0	0	---

PDS_SEQ_DEP
Size 1

PDS Sequential Dependency

USC_SEQ_DEP
Size 1

USC Sequential Dependency

TARGET
Size 1

USC Target (0=All, 1=Any)

UNIFIED_SIZE
Size 6

Unified Size

COMMON_SHARED
Size 1

PDS Common Store Allocation is Shared Registers

COMMON_SIZE
Size 9

PDS Common Size

TEMP_SIZE
Size 4

PDS Temp Size

DATA_SIZE
Size 6

PDS Data Size

FENCE

Size 1

Fence the Task in the PDS/USC - Set on Store, unset on Load

ROGUE_CR_CDM_CONTEXT_STATE_BASE

Size: 48

Address: 0x00000498**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** LLS

Register banks: cdm_dv jones

Kick pipeline: compute_fe

47	46	45	44	43	42	41	40
ADDR (_) ...							

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)	*reserved*						

The base address in external memory of the CDM's context state buffer, to which it will store its snapshot state on a context store and from which it will reload on a context resume.

Name	MSB	LSB	Default	Description	Bank Filter
ADDR	47	7	---	256TB range, 128 byte aligned base address	

ADDR

Size: 41

Type: Define

ALIGN: 7

256TB range, 128 byte aligned base address

ROGUE_CR_CDM_CTRL_STREAM_BASE

Size 40

Address: 0x00000480

Access: read-write

Member of groups: jones tornado hub

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24

ADDR (_) ...

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)						*reserved*	

The base address of the Compute Data Master's Input Parameter Control Stream in external memory

Name	Type	MSB	LSB	Default
ADDR	_	39	2	---

ADDR

Size 38

TB range, 32-bit aligned base address

ROGUE_CR_CDM_ITEM

Size 2

Address: 0x000004c8

Access: read-write

Member of groups: texas3 jones tornado hub

7	6	5	4	3	2	1	0
-						MODE (_) ...	

This register defines the order in which the CDM will output Work Items within a Work group.

Name	MSB	LSB	Default
MODE	1	0	0

MODE

Size 2

00 - FORCE_LINEAR, 01 - RESERVED, 10 - 2D_MORTON, 11 - 3D_MORTON

Possible Values:

Name	Value/Range	Info
FORCE_LINEAR	0 [0]	Linear ordering
2D_MORTON	2 [0x2]	2D Morton ordering
3D_MORTON	3 [0x3]	3D Morton ordering

ROGUE_CR_CDM_TERMINATE_PDS

Size 64

Address: 0x000004b8

Access: read-write

Member of groups: texas3 tornado hub

63	62	61	60	59	58	57	56
DATA_ADDR (_) ...							

55	54	53	52	51	50	49	48
DATA_ADDR (_) ...							

47	46	45	44	43	42	41	40
DATA_ADDR (_) ...							

39	38	37	36	35	34	33	32
DATA_ADDR (_)				*reserved*			

31	30	29	28	27	26	25	24
CODE_ADDR (_) ...							

23	22	21	20	19	18	17	16
CODE_ADDR (_) ...							

15	14	13	12	11	10	9	8
CODE_ADDR (_) ...							

7	6	5	4	3	2	1	0
CODE_ADDR (_)				*reserved*			

This register contains the PDS Code and Data Addresses for the Terminate Program. This program is sent to PDS on Context Store after the Context Store Program

Name	Type	MSB	LSB	Default
DATA_ADDR	_	63	36	---
CODE_ADDR	_	31	4	---

DATA_ADDR

Size 28

PDS Data Address for Terminate Program, 128-bit aligned

CODE_ADDR

Size 28

PDS Code Address for Terminate Program, 128-bit aligned

ROGUE_CR_CDM_TERMINATE_PDS1

Size 30

Address: 0x000004c0

Access: read-write

Member of groups: texas3 tornado hub

31	30	29	28	27	26	25	24
-	PDS_SEQ_DEP (_)		USC_SEQ_DEP (_)		TARGET (_)	UNIFIED_SIZE (_) ...	

23	22	21	20	19	18	17	16
UNIFIED_SIZE (_)			COMMON_SHARED (_)		COMMON_SIZE (_) ...		

15	14	13	12	11	10	9	8

COMMON_SIZE (_)	TEMP_SIZE (_) ...

7	6	5	4	3	2	1	0
TEMP_SIZE (_)	DATA_SIZE (_)						FENCE (_) ...

This register contains the PDS Task Data necessary to produce the Context Store Terminate PDS Program Task from CDM to PDS

Name	Type	MSB	LSB	Default
PDS_SEQ_DEP	_	29	29	---
USC_SEQ_DEP	_	28	28	---
TARGET	_	27	27	---
UNIFIED_SIZE	_	26	21	---
COMMON_SHARED	_	20	20	---
COMMON_SIZE	_	19	11	---
TEMP_SIZE	_	10	7	---
DATA_SIZE	_	6	1	---
FENCE	_	0	0	---

PDS_SEQ_DEP
Size 1

PDS Sequential Dependency

USC_SEQ_DEP
Size 1

USC Sequential Dependency

TARGET
Size 1

USC Target (0=All, 1=Any)

UNIFIED_SIZE
Size 6

Unified Size

COMMON_SHARED
Size 1

PDS Common Store Allocation is Shared Registers

COMMON_SIZE
Size 9

PDS Common Size

TEMP_SIZE
Size 4

PDS Temp Size

DATA_SIZE
Size 6

PDS Data Size

FENCE
Size 1

Fence the Task in the PDS/USC - Set on Store Terminate

ROGUE_CR_COMPUTE_CLUSTER
Size 32

Address: 0x00000068

Access: read-write

Member of groups: jones tornado

31	30	29	28	27	26	25	24
MASK (_) ...							

23	22	21	20	19	18	17	16
MASK (_) ...							

15	14	13	12	11	10	9	8
MASK (_) ...							

7	6	5	4	3	2	1	0
MASK (_) ...							

This mask register enables CDM output to the Clusters present in the design. Resets to a single Cluster being driven with Compute Tasks. To enable Compute processing on more USCs, write this register appropriately. The register should only be programmed with a marching 1's pattern; for example in a 4 Cluster configuration the following values are value: 0x1 - USC0 will process Compute Tasks 0x3 - USC0,1 will process Compute Tasks 0x7 - USC0,1,2 will process Compute Tasks 0xF - USC0,1,2,3 will process Compute Tasks. If the system contains more than 4 Clusters, then higher values are valid to enable Compute processing on those Clusters.

Name	MSB	LSB	Default
MASK	31	0	0xffffffff

MASK
Size 32

A Mask of Clusters enabled for Compute processing. 1 = USC0 only, 3 = USC0&1, 7=USC0,1,2 and 3 etc.

ROGUE_CR_EVENT_PIXEL_PDS_CODE
Size: 36

Address: 0x00000618**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** 3D

Register banks: texas

Kick pipeline: global

39	38	37	36	35	34	33	32
-				*reserved*			

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)				*reserved*			

Name	MSB	LSB	Default	Description	Bank Filter
ADDR	31	4	---	PDS Code segment address for pixel event (control) tasks (Positioned as a byte address, 128 bit granularity), 4 GB Range	

ADDR

Size: 28

Type: Define

ALIGN: 4

PDS Code segment address for pixel event (control) tasks (Positioned as a byte address, 128 bit granularity), 4 GB Range

ROGUE_CR_EVENT_PIXEL_PDS_DATA

Size: 36

Address: 0x00000620**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** 3D

Register banks: texas

Kick pipeline: global

39	38	37	36	35	34	33	32
-				*reserved*			

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)				*reserved*			

Name	MSB	LSB	Default	Description	Bank Filter
ADDR	31	4	---	PDS Data segment (constant) address for pixel event (control) tasks (Positioned as a byte address, 128 bit granularity), 4 GB Range	

ADDR

Size: 28

Type: Define

ALIGN: 4

PDS Data segment (constant) address for pixel event (control) tasks (Positioned as a byte address, 128 bit granularity), 4 GB Range

ROGUE_CR_EVENT_PIXEL_PDS_INFO

Size: 32

Address: 0x00000628**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** 3D

Register banks: texas

Kick pipeline: global

31	30	29	28	27	26	25	24
PDS_SHAREDSIZE (_)					*reserved*		

23	22	21	20	19	18	17	16
reserved		PDS_TEMPSIZE (_)					*reserved*

15	14	13	12	11	10	9	8
reserved							

7	6	5	4	3	2	1	0
reserved	USC_SHAREDSIZE (_) ...						

Name	MSB	LSB	Default	Description	Bank Filter
PDS_SHAREDSIZE	31	27	---	PDS constant data segment size for pixel event (control) tasks in units of 4 DWORDs.	
PDS_TEMPSIZE	21	17	---	PDS temp segment size in units of 2 DWORDs for pixel event (control). Data Size + (Temp Size * Max Insatnces Per Task) < 288 32 bit words. Max instances for pixel event (control) tasks is 1.	
USC_SHAREDSIZE	6	0	---	USC Shared Store allocation size in units of 64 DWORDs for pixel event (control) tasks.	

PDS_SHAREDSIZE

Size: 5

Type: Define

ALIGN: 2

PDS constant data segment size for pixel event (control) tasks in units of 4 DWORDs.

PDS_TEMPSIZE

Size: 5

Type: Define

ALIGN: 1

PDS temp segment size in units of 2 DWORDs for pixel event (control). Data Size + (Temp Size * Max Insatnces Per Task) < 288 32 bit words. Max instances for pixel event (control) tasks is 1.

USC_SHAREDSIZE

Size: 7

Type: Define

ALIGN: 6

USC Shared Store allocation size in units of 64 DWORDs for pixel event (control) tasks.

ROGUE_CR_EVENT_TDM_PDS_CODE

Size: 36

Address: 0x00000900**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** 2D

Register banks: pds_dv texas

Kick pipeline: two_d_be

39	38	37	36	35	34	33	32
-				*reserved*			

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)				*reserved*			

PDS code segment address for 2D End-of-Tile event shader.

Name	MSB	LSB	Default	Description	Bank Filter
ADDR	31	4	---	PDS Code segment address for TDM event (control) tasks (Positioned as a byte address, 128 bit granularity), 4 GB Range	

ADDR

Size: 28

Type: Define

ALIGN: 4

PDS Code segment address for TDM event (control) tasks (Positioned as a byte address, 128 bit granularity), 4 GB Range

ROGUE_CR_EVENT_TDM_PDS_DATA

Size: 36

Address: 0x00000908**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** 2D

Register banks: pds_dv texas

Kick pipeline: two_d_be

39	38	37	36	35	34	33	32
-				*reserved*			

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)				*reserved*			

Name	MSB	LSB	Default	Description	Bank Filter
ADDR	31	4	---	PDS Data segment (constant) address for TDM event (control) tasks (Positioned as a byte address, 128 bit granularity), 4 GB Range	

ADDR
Size: 28

Type: Define

ALIGN: 4

PDS Data segment (constant) address for TDM event (control) tasks (Positioned as a byte address, 128 bit granularity), 4 GB Range

---

ROGUE_CR_EVENT_TDM_PDS_INFO
Size: 32

Address: 0x00000910**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** 2D

Register banks: pds_dv texas

Kick pipeline: two_d_be

31	30	29	28	27	26	25	24
PDS_SHAREDSIZE (_)					*reserved*		

23	22	21	20	19	18	17	16
reserved		PDS_TEMPSIZE (_)					*reserved*

15	14	13	12	11	10	9	8
reserved							

7	6	5	4	3	2	1	0
reserved	USC_SHAREDSIZE (_) ...						

Name	MSB	LSB	Default	Description	Bank Filter
PDS_SHAREDSIZE	31	27	---	PDS constant data segment size for TDM event (control) tasks in units of 4 DWORDs.	
PDS_TEMPSIZE	21	17	---	PDS temp segment size in units of 2 DWORDs for TDM event (control) tasks. Data Size + (Temp Size * Max Insatnces Per Task) < 288 32 bit words. Max instances for pixel event tasks is 1.	
USC_SHAREDSIZE	6	0	---	USC Shared Store allocation size in units of 64 DWORDs for TDM event (control) tasks.	

PDS_SHAREDSIZE
Size: 5

Type: Define

ALIGN: 2

PDS constant data segment size for TDM event (control) tasks in units of 4 DWORDs.

PDS_TEMPSIZE
Size: 5

Type: Define

ALIGN: 1

PDS temp segment size in units of 2 DWORDs for TDM event (control) tasks. Data Size + (Temp Size * Max Insatnces Per Task) < 288 32 bit words. Max instances for pixel event tasks is 1.

USC_SHAREDSIZE

Size: 7

Type: Define

ALIGN: 6

USC Shared Store allocation size in units of 64 DWORDs for TDM event (control) tasks.

ROGUE_CR_FB_CDC_ZLS

Size 43

Address: 0x00001710

Access: read-write

Member of groups: blackpearl texas bifpmcache

47	46	45	44	43	42	41	40
-					*reserved*	FBDC_STENCIL_FMT (_) ...	

39	38	37	36	35	34	33	32
FBDC_STENCIL_FMT (_)						FBDC_DEPTH_FMT (_) ...	

31	30	29	28	27	26	25	24
FBDC_DEPTH_FMT (_)					FBC_NUM_TILES (_) ...		

23	22	21	20	19	18	17	16
FBC_NUM_TILES (_) ...							

15	14	13	12	11	10	9	8
FBC_NUM_TILES (_) ...							

7	6	5	4	3	2	1	0
FBC_NUM_TILES (_)				*reserved*		FBC_IADDR (_)	FBDC_IADDR (_) ...

Framebuffer Compression/Decompression configuration register for ZLS access

Name	MSB	LSB	Default
FBDC_STENCIL_FMT	40	34	0
FBDC_DEPTH_FMT	33	27	0x12
FBC_NUM_TILES	26	4	---
FBC_IADDR	1	1	---
FBDC_IADDR	0	0	---

FBDC_IADDR

Size 1

FBDC Addressing mode 0 = direct ; 1 = indirect

FBC_IADDR

Size 1

FBC Addressing mode 0 = direct ; 1 = indirect

FBC_NUM_TILES
Size 23

FBC ZLS number of compressor tiles in surface, in granularity of 8x8x32dwords

FBDC_DEPTH_FMT
Size 7

ZLS pixel format to use for depth, default F32

FBDC_STENCIL_FMT
Size 7

ZLS pixel format to use for stencil, default U8

ROGUE_CR_FB_MEM_REGION0
Size 57

Address: 0x00001610

Access: read-write

Member of groups: sidekick

63	62	61	60	59	58	57	56
-							NUM_TILES (_) ...

55	54	53	52	51	50	49	48
NUM_TILES (_) ...							

47	46	45	44	43	42	41	40
NUM_TILES (_) ...							

39	38	37	36	35	34	33	32
NUM_TILES (_)						BASE_ADDRESS (_) ...	

31	30	29	28	27	26	25	24
BASE_ADDRESS (_) ...							

23	22	21	20	19	18	17	16
BASE_ADDRESS (_) ...							

15	14	13	12	11	10	9	8
BASE_ADDRESS (_) ...							

7	6	5	4	3	2	1	0
BASE_ADDRESS (_) ...							

Framebuffer Compression/Decompression memory regions for Host and TLA accesses

Name	MSB	LSB	Default
NUM_TILES	56	34	---
BASE_ADDRESS	33	0	---

BASE_ADDRESS
Size 34

Base address of this memory region in 512bit granularity

NUM_TILES
Size 23

The number of compressor tiles to be used in this memory region

---

ROGUE_CR_FB_MEM_REGION1
Size 57

Address: 0x00001618

Access: read-write

Member of groups: sidekick

63	62	61	60	59	58	57	56
-							NUM_TILES (_) ...

55	54	53	52	51	50	49	48
NUM_TILES (_) ...							

47	46	45	44	43	42	41	40
NUM_TILES (_) ...							

39	38	37	36	35	34	33	32
NUM_TILES (_)						BASE_ADDRESS (_) ...	

31	30	29	28	27	26	25	24
BASE_ADDRESS (_) ...							

23	22	21	20	19	18	17	16
BASE_ADDRESS (_) ...							

15	14	13	12	11	10	9	8
BASE_ADDRESS (_) ...							

7	6	5	4	3	2	1	0
BASE_ADDRESS (_) ...							

Framebuffer Compression/Decompression memory regions for Host and TLA accesses

Name	MSB	LSB	Default
NUM_TILES	56	34	---
BASE_ADDRESS	33	0	---

BASE_ADDRESS
Size 34

Base address of this memory region in 512bit granularity

NUM_TILES
Size 23

The number of compressor tiles to be used in this memory region

ROGUE_CR_FB_MEM_REGION_CTRL0

Size 47

Address: 0x00001690

Access: read-write

Member of groups: sidekick

47	46	45	44	43	42	41	40
-	PORT (_)	ACTIVE (_)	SLC_NOLINEFILL (_)	SLC_POLICY (_)		TLCACHE_POLICY (_)	COR_COLOUR_ENABLE (_)

39	38	37	36	35	34	33	32
IADDR (_)	DIMY (_) ...						

31	30	29	28	27	26	25	24
DIMY (_)							DIMX (_) ...

23	22	21	20	19	18	17	16
DIMX (_) ...							

15	14	13	12	11	10	9	8
DIMX (_)				MEML (_)	DM (_)		TILE_TYPE (_)

7	6	5	4	3	2	1	0
FMT (_)							MODE (_) ...

Framebuffer Compression/Decompression memory regions for Host and TLA accesses

Name	MSB	LSB	Default
PORT	46	46	0
ACTIVE	45	45	0
SLC_NOLINEFILL	44	44	---
SLC_POLICY	43	42	---
TLCACHE_POLICY	41	41	---
COR_COLOUR_ENABLE	40	40	---
IADDR	39	39	---
DIMY	38	25	---
DIMX	24	12	---
MEML	11	11	---
DM	10	9	---
TILE_TYPE	8	8	---
FMT	7	1	---
MODE	0	0	0

MODE

Size 1

Defines if this memory region maps to BIF or FBC/FBDC access; 0 = BIF, 1 = FBC/FBDC

FMT

Size 7

The pixel format to be used in this memory region

TILE_TYPE
Size 1

Compressor tile type 0 = 8x8 pixels, 1 = 16x4 pixels

DM
Size 2

Data master to be used for this memory region 00 = TA/Vertex 01 = 3D/Pixel 10 = Compute 11 = Data Master of Requester If the memory region is being accessed by the TLA the data master is set to the TLA data master If the memory region is being accessed by the Host the data master is set to the Host data master

MEML
Size 1

Surface Memory layout for this memory region 0=linear, 1=twiddled

DIMX
Size 13

Surface width in terms of TILE_TYPE for this memory region

DIMY
Size 14

Surface height in terms of TILE_TYPE for this memory region

IADDR
Size 1

Direct/Indirect Addressing: 1=indirect, 0=direct

COR_COLOUR_ENABLE
Size 1

Correlation Colour Enable 0=off, 1=on

TLCACHE_POLICY
Size 1

Tile cache Policy: 1=no line fill on miss, 0=line fill on miss

SLC_POLICY
Size 2

SLC cache Policy: 00=Bypass , 01=Write Back , 10 =Write Through , 11=Cached Read

SLC_NOLINEFILL
Size 1

SLC cache no line fill Policy: 0= line fill on miss , 1=no line fill on miss

ACTIVE
Size 1

Defines if this memory region is active or not, default to INACTIVE. Used in conjuction with MODE field to define if a memory region maps to BIF or FBC /FBDC access. If active, then this region base address is used to check if an access is for the BIF or for the FBC/FBDC. If all the region registers are INACTIVE, then an access defaults to BIF.

PORT

Size 1

Defines if this memory region is to be used by the TLA or Host port. 0 = TLA Port 1 = Host Port

ROGUE_CR_FB_MEM_REGION_CTRL1

Size 47

Address: 0x00001698

Access: read-write

Member of groups: sidekick

47	46	45	44	43	42	41	40
-	PORT (_)	ACTIVE (_)	SLC_NOLINEFILL (_)	SLC_POLICY (_)		TLCACHE_POLICY (_)	COR_COLOUR_ENABLE (_)

39	38	37	36	35	34	33	32
IADDR (_)	DIMY (_) ...						

31	30	29	28	27	26	25	24
DIMY (_)							DIMX (_) ...

23	22	21	20	19	18	17	16
DIMX (_) ...							

15	14	13	12	11	10	9	8
DIMX (_)				MEML (_)	DM (_)		TILE_TYPE (_)

7	6	5	4	3	2	1	0
FMT (_)							MODE (_) ...

Framebuffer Compression/Decompression memory regions for Host and TLA accesses

Name	MSB	LSB	Default
PORT	46	46	0
ACTIVE	45	45	0
SLC_NOLINEFILL	44	44	---
SLC_POLICY	43	42	---
TLCACHE_POLICY	41	41	---
COR_COLOUR_ENABLE	40	40	---
IADDR	39	39	---
DIMY	38	25	---
DIMX	24	12	---
MEML	11	11	---
DM	10	9	---
TILE_TYPE	8	8	---
FMT	7	1	---
MODE	0	0	0

MODE
Size 1

Defines if this memory region maps to BIF or FBC/FBDC access; 0 = BIF, 1 = FBC/FBDC

FMT
Size 7

The pixel format to be used in this memory region

TILE_TYPE
Size 1

Compressor tile type 0 = 8x8 pixels, 1 = 16x4 pixels

DM
Size 2

Data master to be used for this memory region 00 = TA/Vertex 01 = 3D/Pixel 10 = Compute 11 = Data Master of Requester If the memory region is being accessed by the TLA the data master is set to the TLA data master If the memory region is being accessed by the Host the data master is set to the Host data master

MEML
Size 1

Surface Memory layout for this memory region 0=linear, 1=twiddled

DIMX
Size 13

Surface width in terms of TILE_TYPE for this memory region

DIMY
Size 14

Surface height in terms of TILE_TYPE for this memory region

IADDR
Size 1

Direct/Indirect Addressing: 1=indirect, 0=direct

COR_COLOUR_ENABLE
Size 1

Correlation Colour Enable 0=off, 1=on

TLCACHE_POLICY
Size 1

Tile cache Policy: 1=no line fill on miss, 0=line fill on miss

SLC_POLICY
Size 2

SLC cache Policy: 00=Bypass , 01=Write Back , 10 =Write Through , 11=Cached Read

SLC_NOLINEFILL
Size 1

SLC cache no line fill Policy: 0= line fill on miss , 1=no line fill on miss

ACTIVE
Size 1

Defines if this memory region is active or not, default to INACTIVE. Used in conjunction with MODE field to define if a memory region maps to BIF or FBC/FBDC access. If active, then this region base address is used to check if an access is for the BIF or for the FBC/FBDC. If all the region registers are INACTIVE, then an access defaults to BIF.

PORT
Size 1

Defines if this memory region is to be used by the TLA or Host port. 0 = TLA Port 1 = Host Port

---

ROGUE_CR_FRAG_SCREEN
Size: 31

Address: 0x00003e40**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** 3D

Register banks: idec_dv ipp_dv jones isp

Kick pipeline: global

31	30	29	28	27	26	25	24
-	YMAX (_) ...						

23	22	21	20	19	18	17	16
YMAX (_)							

15	14	13	12	11	10	9	8
reserved	XMAX (_) ...						

7	6	5	4	3	2	1	0
XMAX (_) ...							

Define the screen size for fragment processing. Pixels on the screen are numbered (0,0) top left, to (XMAX,YMAX) bottom right.

Name	MSB	LSB	Default	Description	Bank Filter
YMAX	30	16	---	Maximum pixel number in y dimension on screen. Screen height in pixels is YMAX+1. 16K x 16K is the max screen size. I.e. 2^14, bit 15 is always written as 0.	
XMAX	14	0	---	Maximum pixel number in x dimension on screen. Screen width in pixels is XMAX+1. 16K x 16K is the max screen size. I.e. 2^14, bit 15 is always written as 0.	

YMAX
Size: 15

Type: Define

Maximum pixel number in y dimension on screen. Screen height in pixels is YMAX+1. 16K x 16K is the max screen size. I.e. 2^14, bit 15 is always written as 0.

XMAX
Size: 15

Type: Define

Maximum pixel number in x dimension on screen. Screen width in pixels is XMAX+1. 16K x 16K is the max screen size. I.e. 2^14, bit 15 is always written as 0.

ROGUE_CR_ISP_AA

Size 2

Address: 0x00000f30

Access: read-write

Member of groups: texas3 pbe texas sidekick hub usc bifpmcache blackpearl rasterisation

7	6	5	4	3	2	1	0
-						MODE (MODE_TYPE) ... = *AA_NONE*	

Controls whether anti-aliasing is enabled or disabled

Name	Type	MSB	LSB	Default
MODE	MODE_TYPE	1	0	AA_NONE [0]

MODE_TYPE

Size 2

Possible Values:

Name	Value/Range	Info
AA_NONE	0 [0]	enable no anti-aliasing
AA_2X	1 [0x1]	enable 2x anti-aliasing
AA_4X	2 [0x2]	enable 4x anti-aliasing
AA_8X	3 [0x3]	enable 8x anti-aliasing

ROGUE_CR_ISP_BGOBJDEPTH

Size: 32

Address: 0x00000fc8**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** 3D

Register banks: isp_dv isp

Kick pipeline: frag_be

31	30	29	28	27	26	25	24
VALUE (_) ...							

23	22	21	20	19	18	17	16
VALUE (_) ...							

15	14	13	12	11	10	9	8
VALUE (_) ...							

7	6	5	4	3	2	1	0
VALUE (_) ...							

The ISP operates by comparing depth values of incoming objects with the results of previous depth compares, in order to make sure there are no unitialised values at the start of the tile or to cover pixels where there are no objects in the scene a default background object is configured under register control. This register provides the floating point depth value for the hardware background object.

Name	MSB	LSB	Default	Description	Bank Filter

VALUE	31	0	---	Note, the format in this register has to be consistent with the format defined by ZLS_STORE_FORMAT register. If depth buffer is F32, then the value here should be IEEE 754 single precisoin floating point If depth buffer is INT24/INT16,then the value here should be UNORM24/UNORM16 foramt as well. Out of Range value will cause un-defined behavior.	

VALUE

Size: 32

Type: Define

Note, the format in this register has to be consistent with the format defined by ZLS_STORE_FORMAT register. If depth buffer is F32, then the value here should be IEEE 754 single precisoin floating point If depth buffer is INT24/INT16,then the value here should be UNORM24/UNORM16 foramt as well. Out of Range value will cause un-defined behavior.

ROGUE_CR_ISP_BGOBJVALS

Size: 10

Address: 0x00000fd0**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** 3D

Register banks: isp_be_dv isp_dv isp

Kick pipeline: frag_be

15	14	13	12	11	10	9	8
-						ENABLEBGTAG (_)	*reserved*

7	6	5	4	3	2	1	0
STENCIL (_) ...							

This register provides enable, mask and stencil information for the hardware background object.

Name	MSB	LSB	Default	Description	Bank Filter
ENABLEBGTAG	9	9	---	When set to 1, at the start of each tile the ISP tag buffer is initialised with the background object tag (default = 1)	
STENCIL	7	0	---	Hardware background object stencil	

ENABLEBGTAG

Size: 1

Type: Define

When set to 1, at the start of each tile the ISP tag buffer is initialised with the background object tag (default = 1)

STENCIL

Size: 8

Type: Define

Hardware background object stencil

ROGUE_CR_ISP_CTL

This description is for XE cores. For XT cores the fields in the register are different.

Size 32

Address: 0x00000f38

Access: read-write

Member of groups: tornado blackpearl rasterisation

31	30	29	28	27	26	25	24
SKIP_INIT_HDRS (_)	*reserved*		PAIR_TILES_VERT (_)	PAIR_TILES (_)	*reserved*		

23	22	21	20	19	18	17	16
reserved			DBIAS_IS_INT (_)	OVERLAP_CHECK_MODE (_)	PT_UPFRONT_DEPTH_DISABLE (_)	PROCESS_EMPTY_TILES (_)	SAMPLE_POS (_)

15	14	13	12	11	10	9	8
PIPE_ENABLE (PIPE_NUM) = *PIPE_ONE*				*reserved*		VALID_ID (_) ...	

7	6	5	4	3	2	1	0
VALID_ID (_)				UPASS_START (_) ...			

ISP control register. This register contains the PIPE_NUM field which controls the number of tiles in flight within the IPP and IPF. The values to which this register should be set are dependent on not only the number of tiles in flight that are desired, but also the version of the architecture in use. For REL 1,2 Cores, this register can be programmed to values of 0x0-0x2 inclusive enabling 1,2 and 3 tiles in flight for the single ISP in the system. In this system the IPP and IPF are both present in the same layout block. For REL 3,7 Cores, the IPP module is remote from the ISP module as the ISP belongs to the scalable elements in the design. A Cluster Group refers to the 4 USCs in a Phantom Block, which also contains an ISP. 1 Cluster Group = 1 IPP, and 1 ISP, 2 Cluster Groups = 1 IPP and 2 ISPs. The IPP module is configured using the register, and the tiles are split between them via the LSB of the Pipe Identifier. When 2 Cluster Groups (6 or 8 USC clusters) are present, as the value of PIPE_NUM is increased, the tile in flight are spread equally between ISP0 and ISP1, as below 0x0: - ISP0 (1 tile in flight) - ISP1 (Not Used - IDLE Pipe) 0x1: - ISP0 (1 tile in flight) - ISP1 (1 tile in flight) 0x2: - ISP0 (2 tiles in flight) - ISP1 (1 tile in flight) 0x3: - ISP0 (2 tiles in flight) - ISP1 (2 tiles in flight) 0x4: - ISP0 (3 tiles in flight) - ISP1 (2 tiles in flight) 0x5: - ISP0 (3 tiles in flight) - ISP1 (3 tiles in flight) 0x6: - ISP0 (4 tiles in flight) - ISP1 (3 tiles in flight) 0x7: - ISP0 (4 tiles in flight) - ISP1 (4 tiles in flight) Value of 0,2,4,6 should never be use on a 8 USC system, as they result in internal GPU imbalance. When 1 Cluster Group is present (1,2,4 USC clusters) , as the value of PIPE_NUM is increased, the tiles in flight will increase every power of 2, since ISP1 is not present. 0x0: - ISP0 (1 tile in flight) 0x2: - ISP0 (2 tiles in flight) 0x4: - ISP0 (3 tiles in flight) 0x6: - ISP0 (4 tiles in flight) A value which is higher than the number of IPF pipelines will result in the maximum number of pipelines being used. However, the number of pipelines being used should always be less than or equal to the number of tiles which the USC is able to concurrently process (i.e. the number of partitions). In a 4 or 8 cluster system there is 1 partition per tile. In a 2 cluster system there are 2 partitions per tile and in a 1 cluster system there are 4 partitions per tile. Effectively this means this register should be programmed according to the number of partitions available in the USC. NUM_TILES_PER_USC: 00 : 1 tile 01 : 2 tiles in the flight per usc cluster enabled 11 : 2 tiles in the flight per usc cluster enabled

Name	Type	MSB	LSB	Default
SKIP_INIT_HDRS	_	31	31	0
PAIR_TILES_VERT	_	28	28	0
PAIR_TILES	_	27	27	0
DBIAS_IS_INT	_	20	20	0
OVERLAP_CHECK_MODE	_	19	19	0
PT_UPFRONT_DEPTH_DISABLE	_	18	18	0
PROCESS_EMPTY_TILES	_	17	17	0
SAMPLE_POS	_	16	16	---
PIPE_ENABLE	PIPE_NUM	15	12	PIPE_ONE [0]
VALID_ID	_	9	4	---
UPASS_START	_	3	0	---

PIPE_NUM

Size 4

Possible Values:

Name	Value/Range	Info
PIPE_ONE	0 [0]	Rel 1,2: 1 Tile In Flight, others 1 tile-in-flight, for 1 cluster group
PIPE_TWO	1 [0x1]	Rel 1,2: 2 Tiles In Flight, others 1 tile-in-flight, for 2 cluster group
PIPE_THREE	2 [0x2]	Rel 1,2: 3 Tiles In Flight, others 2 tiles-in-flight, for 1 cluster group
PIPE_FOUR	3 [0x3]	2 tiles-in-flight, for 2 cluster group
PIPE_FIVE	4 [0x4]	3 tiles-in-flight, for 1 cluster group
PIPE_SIX	5 [0x5]	3 tiles-in-flight, for 2 cluster group

PIPE_SEVEN	6 [0x6]	4 tiles-in-flight, for 1 cluster group
PIPE_EIGHT	7 [0x7]	4 tiles-in-flight, for 2 cluster group
PIPE_NINE	8 [0x8]	5 tiles-in-flight, for 1 cluster group
PIPE_TEN	9 [0x9]	5 tiles-in-flight, for 2 cluster group
PIPE_ELEVEN	10 [0xa]	6 tiles-in-flight, for 1 cluster group
PIPE_TWELVE	11 [0xb]	6 tiles-in-flight, for 2 cluster group
PIPE_THIRTEEN	12 [0xc]	7 tiles-in-flight, for 1 cluster group
PIPE_FOURTEEN	13 [0xd]	7 tiles-in-flight, for 2 cluster group
PIPE_FIFTEEN	14 [0xe]	8 tiles-in-flight, for 1 cluster group
PIPE_SIXTEEN	15 [0xf]	8 tiles-in-flight, for 2 cluster group

SKIP_INIT_HDRS
Size 1

Used to enable skipping of initial region headers based on gpu offset '0': reads all region headers and discards the ones not needed. '1': skip reading of region headers based on gpu offset

PAIR_TILES_VERT
Size 1

If set, causes IPF to pair tiles vertically within its pipeline.

PAIR_TILES
Size 1

If set, causes IPF to pair tiles within its pipeline.

DBIAS_IS_INT
Size 1

When set, depth bias value is a signed integer

OVERLAP_CHECK_MODE
Size 1

0 - different samples for the same pixel will be sent to different pass groups for translucent objects (pixel to pixel overlap test) 1 - different samples for the same pixel will be sent as the same pass group (sample to sample overlap test)

PT_UPFRONT_DEPTH_DISABLE
Size 1

When set, disable UPFRONT depth test in the Depthsorter

PROCESS_EMPTY_TILES
Size 1

When set empty tiles are always processed rather than being suppressed

SAMPLE_POS
Size 1

Specifies the sampling rule to be used when calculating the endpoint adjustment for thin lines

VALID_ID
Size 6

Triangle validation value

UPASS_START
Size 4

User pass start value

ROGUE_CR_ISP_DBIAS_BASE
Size 40

Address: 0x00000fb8

Access: read-write

Member of groups: blackpearl rasterisation

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)						*reserved*	

Name	Type	MSB	LSB	Default
ADDR	_	39	2	---

ADDR
Size 38

1TB range, 32-bit aligned base address

ROGUE_CR_ISP_MTILE_SIZE
Size 28

Address: 0x00000f18

Access: read-write

Member of groups: jones tornado blackpearl rasterisation

31	30	29	28	27	26	25	24
-				*reserved*		X (_) ...	

23	22	21	20	19	18	17	16
X (_)							

15	14	13	12	11	10	9	8

reserved	Y (_) ...

7	6	5	4	3	2	1	0
Y (_) ...							

Name	Type	MSB	LSB	Default
X	_	25	16	---
Y	_	9	0	---

X
Size 10

Macrotile width, in tiles. A value of zero corresponds to the maximum size

Y
Size 10

Macrotile height, in tiles. A value of zero corresponds to the maximum size

ROGUE_CR_ISP_MTILE_BASE
Size 40

Address: 0x00000f20

Access: read-write

Member of groups: jones tornado blackpearl rasterisation

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)							*reserved*

Name	Type	MSB	LSB	Default
ADDR	_	39	2	---

ADDR
Size 38

1TB range, 32-bit aligned base address

ROGUE_CR_ISP_OCLQRY_BASE
Size 40

Address: 0x00000fc0

Access: read-write

Member of groups: blackpearl rasterisation

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)				*reserved*			

Base address for occlusion query counter values. For multiple phantom system, base address could be set differently and driver needs to sum up the result from different phantoms which have same occlusion query index.

Name	Type	MSB	LSB	Default
ADDR	_	39	4	---

ADDR

Size 36

1TB range, 128-bit aligned base address

ROGUE_CR_ISP_RENDER

Size 9

Address: 0x00000f08

Access: read-write

Member of groups: texas jones tornado bifpmcache blackpearl rasterisation

15	14	13	12	11	10	9	8
-							FAST_RENDER_FORCE_PROTECT (_)

7	6	5	4	3	2	1	0
PROCESS_PROTECTED_TILES (_)	PROCESS_UNPROTECTED_TILES (_)	DISABLE_EOMT (_)	RESUME (_)	DIR (DIR_TYPE) = *TL2BR*		MODE (MODE_TYPE) ... = *NORM*	

Controls the render

Name	Type	MSB	LSB	Default
FAST_RENDER_FORCE_PROTECT	_	8	8	0
PROCESS_PROTECTED_TILES	_	7	7	0
PROCESS_UNPROTECTED_TILES	_	6	6	0
DISABLE_EOMT	_	5	5	0
RESUME	_	4	4	---
DIR	DIR_TYPE	3	2	TL2BR [0]
MODE	MODE_TYPE	1	0	NORM [0]

DIR_TYPE

Size 2

Possible Values:

Name	Value/Range	Info
TL2BR	0 [0]	Top-left to bottom-right
TR2BL	1 [0x1]	Top-right to bottom-left
BL2TR	2 [0x2]	Bottom-left to top-right
BR2TL	3 [0x3]	Bottom-right to top-left

MODE_TYPE
Size 2

Possible Values:

Name	Value/Range	Info
NORM	0 [0]	Normal render
FAST_2D	2 [0x2]	Fast 2D render
FAST_SCALE	3 [0x3]	Fast scale render

FAST_RENDER_FORCE_PROTECT
Size 1

When set, all tiles to be rasterised are marked as protected

PROCESS_PROTECTED_TILES
Size 1

When set, protected tiles are processed

PROCESS_UNPROTECTED_TILES
Size 1

When set, unprotected tiles are processed

DISABLE_EOMT
Size 1

Prevent End-of-Macro-Tile flags being sent to ISP

RESUME
Size 1

Render resume

ROGUE_CR_ISP_RENDER_ORIGIN
Size 26

Address: 0x00000f10

Access: read-write

Member of groups: jones tornado blackpearl rasterisation

31	30	29	28	27	26	25	24
-						X (_) ...	

23	22	21	20	19	18	17	16
X (_)							

15	14	13	12	11	10	9	8
reserved						Y (_) ...	

7	6	5	4	3	2	1	0
Y (_) ...							

This register defines the top-left tile coordinate for the render.

Name	Type	MSB	LSB	Default
X	_	25	16	---
Y	_	9	0	---

X

Size 10

X coordinate, in tiles

Y

Size 10

Y coordinate, in tiles

ROGUE_CR_ISP_RGN

Size 30

Address: 0x00000f28

Access: read-write

Member of groups: rasterisation

31	30	29	28	27	26	25	24
-	*reserved*		CS_SIZE (_)				

23	22	21	20	19	18	17	16
SIZE (_) ...							

15	14	13	12	11	10	9	8
SIZE (_) ...							

7	6	5	4	3	2	1	0
SIZE (_) ...							

This register defines the sizes of the allocations of the simple internal parameter data.

Name	Type	MSB	LSB	Default
CS_SIZE	_	28	24	0x1f
SIZE	_	23	0	---

CS_SIZE

Size 5

Number of primitive headers in the control stream for a fast 2D render. If the number of primitive headers exceeds the maximum field size or the size of the control stream is unknown, a value of all ones should be written

SIZE

Size 24

Number of Region Headers to fetch

ROGUE_CR_ISP_SCISSOR_BASE

Size 40

Address: 0x00000fb0

Access: read-write

Member of groups: blackpearl rasterisation

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)						*reserved*	

Name	Type	MSB	LSB	Default
ADDR	_	39	2	---

ADDR

Size 38

1TB range, 32-bit aligned base address

ROGUE_CR_ISP_STENCIL_LOAD_BASE

Size 40

Address: 0x00000f60

Access: read-write

Member of groups: blackpearl texas bifpmcache rasterisation

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)				*reserved*			ENABLE (_) ...

Base address in memory of the Stencil Buffer base address to load into the ISP for non-compressed ZLS formats. This alternate stencil buffer base address is selectable based on the enable bit.

Name	Type	MSB	LSB	Default
ADDR	_	39	4	---
ENABLE	_	0	0	---

ADDR

Size 36

1TB Addressable, 16byte aligned Base Address of the Z Buffer Load base address

ENABLE

Size 1

When set to 1, enables fetching of stencil from a separate base address

ROGUE_CR_ISP_STENCIL_STORE_BASE

Size 40

Address: 0x00000f68

Access: read-write

Member of groups: blackpearl texas bifpmcache rasterisation

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)				*reserved*			ENABLE (_) ...

Base address in memory of the Stencil Buffer base address to store into the ISP for non-compressed ZLS formats. This alternate stencil buffer base address is selectable based on the enable bit.

Name	Type	MSB	LSB	Default
ADDR	_	39	4	---
ENABLE	_	0	0	---

ADDR

Size 36

1TB Addressable, 16byte aligned Base Address of the Z Buffer Load base address

ENABLE

Size 1

When set to 1, enables fetching of stencil from a separate base address

ROGUE_CR_ISP_STORE0

Size 31

Address: 0x00001008

Access: readonly

Member of groups: tornado rasterisation

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved		TILE_X (_) ...					

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE1

Size 31

Address: 0x00001010

Access: readonly

Member of groups: tornado rasterisation

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved	TILE_X (_) ...						

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE2
Size 31

Address: 0x00001018

Access: readonly

Member of groups: tornado rasterisation

31	30	29	28	27	26	25	24

-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)

23	22	21	20	19	18	17	16
reserved		TILE_X (_) ...					

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE3
Size 31

Address: 0x00001060

Access: readonly

Member of groups: rasterisation tornado

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved		TILE_X (_) ...					

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE4
Size 31

Address: 0x00001068

Access: readonly

Member of groups: rasterisation tornado

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved		TILE_X (_) ...					

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE5
Size 31

Address: 0x00001070

Access: readonly

Member of groups: rasterisation tornado

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved	TILE_X (_) ...						

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE6
Size 31

Address: 0x000010a0

Access: readonly

Member of groups: rasterisation tornado

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved		TILE_X (_) ...					

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---

TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE7
Size 31

Address: 0x000010a8

Access: readonly

Member of groups: rasterisation tornado

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved	TILE_X (_) ...						

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE8
Size 31

Address: 0x000010c0

Access: readonly

Member of groups: rasterisation

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved	TILE_X (_) ...						

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE9
Size 31

Address: 0x000010c8

Access: readonly

Member of groups: rasterisation

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved	TILE_X (_) ...						

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE10
Size 31

Address: 0x000010d0

Access: readonly

Member of groups: rasterisation

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved	TILE_X (_) ...						

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE11
Size 31

Address: 0x000010d8

Access: readonly

Member of groups: rasterisation

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved	TILE_X (_) ...						

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE12
Size 31

Address: 0x000010e0

Access: readonly

Member of groups: rasterisation

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved	TILE_X (_) ...						

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE13
Size 31

Address: 0x000010e8

Access: readonly

Member of groups: rasterisation

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved	TILE_X (_) ...						

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_STORE14

Size 31

Address: 0x000010f0

Access: readonly

Member of groups: rasterisation

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved	TILE_X (_) ...						

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE

Size 1

EOR

Size 1

TILE_LAST

Size 1

MT

Size 4

TILE_X

Size 10

TILE_Y

Size 10

ROGUE_CR_ISP_STORE15

Size 31

Address: 0x000010f8

Access: readonly

Member of groups: rasterisation

31	30	29	28	27	26	25	24
-	ACTIVE (_)	EOR (_)	TILE_LAST (_)	MT (_)			

23	22	21	20	19	18	17	16
reserved	TILE_X (_) ...						

15	14	13	12	11	10	9	8
TILE_X (_)				*reserved*		TILE_Y (_) ...	

7	6	5	4	3	2	1	0
TILE_Y (_) ...							

ISP context store register

Name	MSB	LSB	Default
ACTIVE	30	30	---
EOR	29	29	---
TILE_LAST	28	28	---
MT	27	24	---
TILE_X	21	12	---
TILE_Y	9	0	---

ACTIVE
Size 1

EOR
Size 1

TILE_LAST
Size 1

MT
Size 4

TILE_X
Size 10

TILE_Y
Size 10

ROGUE_CR_ISP_XTP_PIPE_ENABLE
Size 33

Address: 0x00003e00

Access: read-write

Member of groups: jones

39	38	37	36	35	34	33	32

-	*reserved*

31	30	29	28	27	26	25	24
reserved				CORE3_COUNT (_)			

23	22	21	20	19	18	17	16
reserved				CORE2_COUNT (_)			

15	14	13	12	11	10	9	8
reserved				CORE1_COUNT (_)			

7	6	5	4	3	2	1	0
reserved				CORE0_COUNT (_) ...			

ISP XT+ control register for the number of tiles being processed in each rasterisation module. There is 1 rasterisation module for every 4 clusters. Where there is a non multiple of 4 clusters round up to the next multiple of 4. The count field is per rasterisation module, and there is a maximum of 4 rasterisation modules. A value which is higher than the number of IPF pipelines will result in the maximum number of pipelines being used. However, the number of pipeline being used should always be less than or equal to the number of tiles which the USC is able to concurrently process (i.e. the number of partitions). There are X (2) tiles per USC. On a 2 cluster system then count 0 would be 4. In a 6 cluster system count 0 would be 8 and count 1 would be 4.

Name	MSB	LSB	Default
CORE3_COUNT	28	24	0x1f
CORE2_COUNT	20	16	0x1f
CORE1_COUNT	12	8	0x1f
CORE0_COUNT	4	0	0x1f

CORE0_COUNT
Size 5

Count of the number of IPF Pipelines to enable for Core 0

CORE1_COUNT
Size 5

Count of the number of IPF Pipelines to enable for Core 1

CORE2_COUNT
Size 5

Count of the number of IPF Pipelines to enable for Core 2

CORE3_COUNT
Size 5

Count of the number of IPF Pipelines to enable for Core 3

ROGUE_CR_ISP_ZLOAD_BASE
Size 40

Address: 0x00000f50

Access: read-write

Member of groups: blackpearl texas bifpmcache rasterisation

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)				*reserved*			

Base address in memory of the Z Buffer base address to load into the ISP for non-compressed ZLS formats.

Name	Type	MSB	LSB	Default
ADDR	_	39	4	---

ADDR

Size 36

1TB Addressable, 16byte aligned Base Address of the Z Buffer Load base address

---

ROGUE_CR_ISP_ZLSCTL

Size 61

Address: 0x00000f48

Access: read-write

Member of groups: jones texas bifpmcache blackpearl rasterisation

63	62	61	60	59	58	57	56
-		*reserved*				ZLSEXTENT_Y_S (_) ...	

55	54	53	52	51	50	49	48
ZLSEXTENT_Y_S (_)							

47	46	45	44	43	42	41	40
ZLSEXTENT_X_S (_) ...							

39	38	37	36	35	34	33	32
ZLSEXTENT_X_S (_)		STENCIL_EXTENT_ENABLE (_)			ZLSEXTENT_Y_Z (_) ...		

31	30	29	28	27	26	25	24
ZLSEXTENT_Y_Z (_)					ZSTOREFORMAT (ZSTOREFORMAT_TYPE)		ZLOADFORMAT (ZLOADFORMAT_TYPE) ...

23	22	21	20	19	18	17	16
ZLOADFORMAT (ZLOADFORMAT_TYPE)							

15	14	13	12	11	10	9	8
ZLOADEN (_)		SLOADEN (_)		LOADTWIDDLED (_)		ZLSEXTENT_X_Z (_) ...	

7	6	5	4	3	2	1	0
ZLSEXTENT_X_Z (_)				FORCEZSTORE (_)		FORCEZLOAD (_)	ZONLYRENDER (_) ...

ISP Z Load/Store & format global control register

Name	Type	MSB	LSB	Default

ZLSEXTENT_Y_S	_	57	48	---
ZLSEXTENT_X_S	_	47	38	---
STENCIL_EXTENT_ENABLE	_	37	37	0
ZLSEXTENT_Y_Z	_	36	27	---
ZSTOREFORMAT	ZSTOREFORMAT_TYPE	26	25	---
ZLOADFORMAT	ZLOADFORMAT_TYPE	24	23	---
FB_STOREEN	_	22	22	---
FB_LOADEN	_	21	21	---
MSTOREEN	_	20	20	---
ZSTOREEN	_	19	19	---
SSTOREEN	_	18	18	---
STORETWIDDLED	_	17	17	---
MLOADEN	_	16	16	---
ZLOADEN	_	15	15	---
SLOADEN	_	14	14	---
LOADTWIDDLED	_	13	13	---
ZLSEXTENT_X_Z	_	12	3	---
FORCEZSTORE	_	2	2	---
FORCEZLOAD	_	1	1	---
ZONLYRENDER	_	0	0	---

ZLSEXTENT_Y_S
Size 10

For stencil buffer, the value calculation is the same as ZLSEXTENT_Y_Z

ZLSEXTENT_X_S
Size 10

For stencil buffer, the value calculation is the same as ZLSEXTENT_X_Z

STENCIL_EXTENT_ENABLE
Size 1

When this bit is '1', stencil buffer will use zlsextent_x/y_s value to calculate zload/store address, otherwise, zlsextent_x/y_z value will be used. The default value is '0' which disables this new function.

ZLSEXTENT_Y_Z
Size 10

For Depth buffer Display width of Y in tiles minus one: 0x000 1 tile, 0x001 2 tiles, .. , 0x2FF 1024 tiles, zlsextent_y = total_samples_y / 32 samples in non-msaa, 4xmsaa mode = total_samples_y / 64 samples in 2xmsaa, 8xmsaa mode. In strided mode, zlsextent_y is set up to above result. In twiddled mode, zlsextent_y uses above result and rounds the value up to the nearest value which is power of 2.

ZSTOREFORMAT_TYPE
Size 2

Possible Values:

Name	Value/Range	Info
F32Z	0 [0]	31 bit IEEE SP Float + 1-bit mask
24BITINT	1 [0x1]	24 bit Integer + 8-bit Stencil
16BITINT	2 [0x2]	16 bit Integer + 8-bit Stencil

F64Z	3 [0x3]	31 bit IEEE SP Float + 1-bit mask + 8-bit Stencil + 24-bit '0's

ZLOADFORMAT_TYPE
Size 2

Possible Values:

Name	Value/Range	Info
F32Z	0 [0]	31 bit IEEE SP Float + 1-bit mask
24BITINT	1 [0x1]	24 bit Integer + 8-bit Stencil
16BITINT	2 [0x2]	16 bit Integer + 8-bit Stencil
F64Z	3 [0x3]	31 bit IEEE SP Float + 1-bit mask + 8-bit Stencil + 24-bit '0's

FB_STOREEN
Size 1

when set, frame buffer compression store is enabled

FB_LOADEN
Size 1

when set, frame buffer decompression load is enabled

MSTOREEN
Size 1

When set and ZSTOREFORMAT = 0x0, mask plane is stored within msb of IEEE format, when set and ZSTOREFORMAT = 0x3, mask plane is stored at bit position 31 of IEEE format, when set for other format, if mask_store_base_enable = '1', background object mask data '0' is stored into separate memory address, when set for other format, if mask_store_base_enable = '0', mask data '0' is stored into separate meory address

ZSTOREEN
Size 1

When set to 1, if the ZSTORE bit in the region header is also set then the depth buffer is stored to memory after each tile is processed

SSTOREEN
Size 1

When set to 1, if the ZSTORE bit in the region header is also set then the stencil buffer is stored to memory after each tile is processed

STORETWIDDLED
Size 1

When set to 1 depth and stencil data is written out in "Twiddled" order.

MLOADEN
Size 1

When set and ZLOADFORMAT = 0x0, mask plane is loaded from msb of IEEE format, when set and ZLOADFORMAT = 0x3, mask plane is loaded from the bit position 31 of IEEE format, when set for other format, if mask_load_base_enable = '1', mask plane is loaded from separate memory address, when set for other format, if mask_load_base_enable = '0', background object mask data is used

ZLOADEN
Size 1

When set to 1, if the ZLOAD bit in the region header is also set then the depth buffer is read from memory prior to tile processing

SLOADEN
Size 1

When set to 1, if the ZLOAD bit in the region header is also set then the stencil buffer is read from memory prior to tile processing

LOADTWIDDLED
Size 1

When set to 1 depth, stencil data is loaded in "Twiddled" order

ZLSEXTENT_X_Z
Size 10

For depth buffer, Display width of X in tiles minus one: 0x000 1 tile, 0x001 2 tiles, .. , 0x2FF 1024 tiles. For different msaa mode, 1xmsaa = 1 x (32,32) pixels = 32x1 x 32x1 = 1024 samples = 32 x 32 samples, 2xmsaa = 2 x (32,32) pixels = 32x1 x 32x2 = 2048 samples = 32 x 64 samples, 4xmsaa = 4 x (32,16) pixels = 32x2 x 16x2 = 2048 samples = 64 x 32 samples, 8xmsaa = 8 x (16,16) pixels = 16x2 x 16x4 = 2048 samples = 32 x 64 samples, So zlsextent_x = total_samples_x / 32 samples when non-msaa, 2xmsaa, 8xmsaa zlsextent_x = total_samples_x / 64 samples when 4xmsaa In strided mode, zlsextent_x is set up to above result. In twiddled mode, zlsextent_x uses above result and rounds the value up to the neareast value which is power of 2.

FORCEZSTORE
Size 1

If set to 1 the depth/stencil buffer is always stored at the end of each tile irrespective of the region header ZSTORE bit.

FORCEZLOAD
Size 1

If set to 1 the depth/stencil buffer is always loaded at the start of each tile irrespective of the region header ZLOAD bit.

ZONLYRENDER
Size 1

When set, only the Z buffer is rendered. Opaque and translucent objects are stencil and depth tested as usual but no pixel spans are emitted to the PDS Pixel presenter. Pixels within punch through and depth feedback objects are emitted on their first pass as a result of passing the up-front depth test by default. However, on their feedback depth test, these pixels will not be output regardless of the depth test result. The intention is to calculate a scene Z buffer without doing any further rendering.

ROGUE_CR_ISP_ZLS_PIXELS
Size 30

Address: 0x00000fd0

Access: read-write

Member of groups: blackpearl rasterisation

31	30	29	28	27	26	25	24
-		Y (_) ...					

23	22	21	20	19	18	17	16
Y (_) ...							

15	14	13	12	11	10	9	8
Y (_)	X (_) ...						

7	6	5	4	3	2	1	0
X (_) ...							

screen size in pixel numbers for ZLS.

Name	Type	MSB	LSB	Default
Y	_	29	15	---
X	_	14	0	---

Y
Size 15

Display width of Y in pixels minus one. 0x000 1 pixel, 0x001 2 pixels, ..., 0x7FFF 1024*32 pixels. Subtile only supports for non-msaa mode depth load /store, so For non-msaa mode, if framebuffer compression, or separate mask or separate stencil is enabled, [4 .. 0] has to be set to x"1F". For 2xmsaa mode, [4 .. 0] has to be set to x"1F". For 4xmsaa mode, [3 .. 0] has to be set to x"F". For 8xmsaa mode, [3 .. 0] has to be set to x"F".

X
Size 15

Display width of X in pixels minus one. 0x000 1 pixel, 0x001 2 pixels, ..., 0x7FFF 1024*32 pixels. Subtile only supports for non-msaa mode depth load /store, so For non-msaa mode, if framebuffer compression, or separate mask or separate stencil is enabled, [4 .. 0] has to be set to x"1F". For 2xmsaa mode, [4 .. 0] has to be set to x"1F". For 4xmsaa mode, [4 .. 0] has to be set to x"1F". For 8xmsaa mode, [3 .. 0] has to be set to x"F".

ROGUE_CR_ISP_ZSTORE_BASE
Size 40

Address: 0x00000f58

Access: read-write

Member of groups: blackpearl texas bifpmcache rasterisation

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)				*reserved*			

Base address in memory of the Z Buffer base address to store into the ISP for non-compressed ZLS formats.

Name	Type	MSB	LSB	Default
ADDR	_	39	4	---

ADDR
Size 36

1TB Addressable, 16byte aligned Base Address of the Z Buffer Store base address

ROGUE_CR_PBE_WORD0_MRT0
Size 64

Address: 0x00001510

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
TFBC_LOSSY	COMPRESS_SIZE_EXT	PAIR_TILES	X_RSRVD2 (_)	DITHER (_)	TILERELATIVE (_)	DOWNSCALE (_)	

55	54	53	52	51	50	49	48
SIZE_Z (SIZE)				ROTATION (ROTATION_TYPE)		LINESTRIDE (_) ...	

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)						MEMLAYOUT	

31	30	29	28	27	26	25	24
SWIZ_CHAN3 (SWIZ)			SWIZ_CHAN2 (SWIZ)			SWIZ_CHAN1 (SWIZ) ...	

23	22	21	20	19	18	17	16
SWIZ_CHAN1 (SWIZ)		SWIZ_CHAN0 (SWIZ)		MINCLIP_X (MINCLIP) ...			

15	14	13	12	11	10	9	8
MINCLIP_X (MINCLIP) ...							

7	6	5	4	3	2	1	0
MINCLIP_X (MINCLIP)		TWOCOMP_GAMMA	GAMMA (_)	COMPRESSION	COMPRESS_SIZE	COMP_INDIRECT_TABLE (_)	Y_FLIP ...

Pixel Back end State Word 0.

Name	Type	MSB	LSB	Default
TFBC_LOSSY	TFBC_LOSSY	63	62	---
COMPRESS_SIZE_EXT	COMPRESS_SIZE_EXT	61	61	---
PAIR_TILES	PAIR_TILES	60	60	---
X_RSRVD2	_	59	59	---
DITHER	_	58	58	---
TILERELATIVE	_	57	57	---
DOWNSCALE	_	56	56	---
SIZE_Z	SIZE	55	52	---
ROTATION	ROTATION_TYPE	51	50	---
LINESTRIDE	_	49	34	---
MEMLAYOUT	MEMLAYOUT	33	32	---
SWIZ_CHAN3	SWIZ	31	29	---
SWIZ_CHAN2	SWIZ	28	26	---
SWIZ_CHAN1	SWIZ	25	23	---
SWIZ_CHAN0	SWIZ	22	20	---
MINCLIP_X	MINCLIP	19	6	---
TWOCOMP_GAMMA	TWOCOMP_GAMMA	5	5	---
GAMMA	_	4	4	---
COMPRESSION	COMPRESSION	3	3	---
COMPRESS_SIZE	COMPRESS_SIZE	2	2	---
COMP_INDIRECT_TABLE	_	1	1	---
Y_FLIP	Y_FLIP	0	0	---

X_RSRVD2
Size 1

Not used

DITHER
Size 1

Enable dither

TILERELATIVE
Size 1

Add tile offset

DOWNSCALE
Size 1

Perform box filter downscale

LINESTRIDE
Size 16

Linestride in 2 pixel units. 0 == 2. Supports 32KDWORD stride memory write

GAMMA
Size 1

Gamma enabled

COMP_INDIRECT_TABLE
Size 1

If set indicates to the compressor that an indirect addressing is used otherwise direct addressing

---

ROGUE_CR_PBE_WORD0_MRT1
Size 64

Address: 0x00001518

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
TFBC_LOSSY	COMPRESS_SIZE_EXT		PAIR_TILES	X_RSRVD2 (_)	DITHER (_)	TILERELATIVE (_)	DOWNSCALE (_)

55	54	53	52	51	50	49	48
SIZE_Z (SIZE)				ROTATION (ROTATION_TYPE)		LINESTRIDE (_) ...	

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)						MEMLAYOUT	

31	30	29	28	27	26	25	24
SWIZ_CHAN3 (SWIZ)			SWIZ_CHAN2 (SWIZ)			SWIZ_CHAN1 (SWIZ) ...	

23	22	21	20	19	18	17	16
SWIZ_CHAN1 (SWIZ)	SWIZ_CHAN0 (SWIZ)	MINCLIP_X (MINCLIP) ...					

15	14	13	12	11	10	9	8
MINCLIP_X (MINCLIP) ...							

7	6	5	4	3	2	1	0
MINCLIP_X (MINCLIP)	TWOCOMP_GAMMA	GAMMA (_)	COMPRESSION	COMPRESS_SIZE	COMP_INDIRECT_TABLE (_)	Y_FLIP ...	

Pixel Back end State Word 0.

Name	Type	MSB	LSB	Default
TFBC_LOSSY	TFBC_LOSSY	63	62	---
COMPRESS_SIZE_EXT	COMPRESS_SIZE_EXT	61	61	---
PAIR_TILES	PAIR_TILES	60	60	---
X_RSRVD2	_	59	59	---
DITHER	_	58	58	---
TILERELATIVE	_	57	57	---
DOWNSCALE	_	56	56	---
SIZE_Z	SIZE	55	52	---
ROTATION	ROTATION_TYPE	51	50	---
LINESTRIDE	_	49	34	---
MEMLAYOUT	MEMLAYOUT	33	32	---
SWIZ_CHAN3	SWIZ	31	29	---
SWIZ_CHAN2	SWIZ	28	26	---
SWIZ_CHAN1	SWIZ	25	23	---
SWIZ_CHAN0	SWIZ	22	20	---
MINCLIP_X	MINCLIP	19	6	---
TWOCOMP_GAMMA	TWOCOMP_GAMMA	5	5	---
GAMMA	_	4	4	---
COMPRESSION	COMPRESSION	3	3	---
COMPRESS_SIZE	COMPRESS_SIZE	2	2	---
COMP_INDIRECT_TABLE	_	1	1	---
Y_FLIP	Y_FLIP	0	0	---

X_RSRVD2

Size 1

Not used

DITHER

Size 1

Enable dither

TILERELATIVE

Size 1

Add tile offset

DOWNSCALE
Size 1

Perform box filter downscale

LINESTRIDE
Size 16

Linestride in 2 pixel units. 0 == 2. Supports 32KDWORD stride memory write

GAMMA
Size 1

Gamma enabled

COMP_INDIRECT_TABLE
Size 1

If set indicates to the compressor that an indirect addressing is used otherwise direct addressing

---

ROGUE_CR_PBE_WORD0_MRT2
Size 64

Address: 0x00001520

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
TFBC_LOSSY	COMPRESS_SIZE_EXT		PAIR_TILES	X_RSRVD2 (_)	DITHER (_)	TILERELATIVE (_)	DOWNSCALE (_)

55	54	53	52	51	50	49	48
SIZE_Z (SIZE)				ROTATION (ROTATION_TYPE)		LINESTRIDE (_) ...	

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)						MEMLAYOUT	

31	30	29	28	27	26	25	24
SWIZ_CHAN3 (SWIZ)			SWIZ_CHAN2 (SWIZ)			SWIZ_CHAN1 (SWIZ) ...	

23	22	21	20	19	18	17	16
SWIZ_CHAN1 (SWIZ)			SWIZ_CHAN0 (SWIZ)			MINCLIP_X (MINCLIP) ...	

15	14	13	12	11	10	9	8
MINCLIP_X (MINCLIP) ...							

7	6	5	4	3	2	1	0
MINCLIP_X (MINCLIP)	TWOCOMP_GAMMA	GAMMA (_)	COMPRESSION	COMPRESS_SIZE	COMP_INDIRECT_TABLE (_)	Y_FLIP ...	

Pixel Back end State Word 0.

Name	Type	MSB	LSB	Default
TFBC_LOSSY	TFBC_LOSSY	63	62	---

COMPRESS_SIZE_EXT	COMPRESS_SIZE_EXT	61	61	---
PAIR_TILES	PAIR_TILES	60	60	---
X_RSRVD2	_	59	59	---
DITHER	_	58	58	---
TILERELATIVE	_	57	57	---
DOWNSCALE	_	56	56	---
SIZE_Z	SIZE	55	52	---
ROTATION	ROTATION_TYPE	51	50	---
LINESTRIDE	_	49	34	---
MEMLAYOUT	MEMLAYOUT	33	32	---
SWIZ_CHAN3	SWIZ	31	29	---
SWIZ_CHAN2	SWIZ	28	26	---
SWIZ_CHAN1	SWIZ	25	23	---
SWIZ_CHAN0	SWIZ	22	20	---
MINCLIP_X	MINCLIP	19	6	---
TWOCOMP_GAMMA	TWOCOMP_GAMMA	5	5	---
GAMMA	_	4	4	---
COMPRESSION	COMPRESSION	3	3	---
COMPRESS_SIZE	COMPRESS_SIZE	2	2	---
COMP_INDIRECT_TABLE	_	1	1	---
Y_FLIP	Y_FLIP	0	0	---

X_RSRVD2
Size 1

Not used

DITHER
Size 1

Enable dither

TILERELATIVE
Size 1

Add tile offset

DOWNSCALE
Size 1

Perform box filter downscale

LINESTRIDE
Size 16

Linestride in 2 pixel units. 0 == 2. Supports 32KDWORD stride memory write

GAMMA
Size 1

Gamma enabled

COMP_INDIRECT_TABLE

Size 1

If set indicates to the compressor that an indirect addressing is used otherwise direct addressing

ROGUE_CR_PBE_WORD0_MRT3

Size 64

Address: 0x00001528

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
TFBC_LOSSY		COMPRESS_SIZE_EXT	PAIR_TILES	X_RSRVD2 (_)	DITHER (_)	TILERELATIVE (_)	DOWNSCALE (_)

55	54	53	52	51	50	49	48
SIZE_Z (SIZE)				ROTATION (ROTATION_TYPE)		LINESTRIDE (_) ...	

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)						MEMLAYOUT	

31	30	29	28	27	26	25	24
SWIZ_CHAN3 (SWIZ)			SWIZ_CHAN2 (SWIZ)			SWIZ_CHAN1 (SWIZ) ...	

23	22	21	20	19	18	17	16
SWIZ_CHAN1 (SWIZ)		SWIZ_CHAN0 (SWIZ)		MINCLIP_X (MINCLIP) ...			

15	14	13	12	11	10	9	8
MINCLIP_X (MINCLIP) ...							

7	6	5	4	3	2	1	0
MINCLIP_X (MINCLIP)	TWOCOMP_GAMMA		GAMMA (_)	COMPRESSION	COMPRESS_SIZE	COMP_INDIRECT_TABLE (_)	Y_FLIP ...

Pixel Back end State Word 0.

Name	Type	MSB	LSB	Default
TFBC_LOSSY	TFBC_LOSSY	63	62	---
COMPRESS_SIZE_EXT	COMPRESS_SIZE_EXT	61	61	---
PAIR_TILES	PAIR_TILES	60	60	---
X_RSRVD2	_	59	59	---
DITHER	_	58	58	---
TILERELATIVE	_	57	57	---
DOWNSCALE	_	56	56	---
SIZE_Z	SIZE	55	52	---
ROTATION	ROTATION_TYPE	51	50	---
LINESTRIDE	_	49	34	---
MEMLAYOUT	MEMLAYOUT	33	32	---
SWIZ_CHAN3	SWIZ	31	29	---
SWIZ_CHAN2	SWIZ	28	26	---
SWIZ_CHAN1	SWIZ	25	23	---

SWIZ_CHAN0	SWIZ	22	20	---
MINCLIP_X	MINCLIP	19	6	---
TWOCOMP_GAMMA	TWOCOMP_GAMMA	5	5	---
GAMMA	_	4	4	---
COMPRESSION	COMPRESSION	3	3	---
COMPRESS_SIZE	COMPRESS_SIZE	2	2	---
COMP_INDIRECT_TABLE	_	1	1	---
Y_FLIP	Y_FLIP	0	0	---

X_RSRVD2
Size 1

Not used

DITHER
Size 1

Enable dither

TILERELATIVE
Size 1

Add tile offset

DOWNSCALE
Size 1

Perform box filter downscale

LINESTRIDE
Size 16

Linestride in 2 pixel units. 0 == 2. Supports 32KDWORD stride memory write

GAMMA
Size 1

Gamma enabled

COMP_INDIRECT_TABLE
Size 1

If set indicates to the compressor that an indirect addressing is used otherwise direct addressing

ROGUE_CR_PBE_WORD0_MRT4
Size 64

Address: 0x00001530

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
TFBC_LOSSY	COMPRESS_SIZE_EXT	PAIR_TILES	X_RSRVD2 (_)	DITHER (_)	TILERELATIVE (_)	DOWNSCALE (_)	

55	54	53	52	51	50	49	48

SIZE_Z (SIZE)				ROTATION (ROTATION_TYPE)		LINESTRIDE (_) ...	

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)						MEMLAYOUT	

31	30	29	28	27	26	25	24
SWIZ_CHAN3 (SWIZ)			SWIZ_CHAN2 (SWIZ)			SWIZ_CHAN1 (SWIZ) ...	

23		22	21	20	19	18	17	16
SWIZ_CHAN1 (SWIZ)		SWIZ_CHAN0 (SWIZ)			MINCLIP_X (MINCLIP) ...			

15	14	13	12	11	10	9	8
MINCLIP_X (MINCLIP) ...							

7	6	5	4	3	2	1	0
MINCLIP_X (MINCLIP)	TWOCOMP_GAMMA	GAMMA (_)	COMPRESSION	COMPRESS_SIZE	COMP_INDIRECT_TABLE (_)	Y_FLIP ...	

Pixel Back end State Word 0.

Name	Type	MSB	LSB	Default
TFBC_LOSSY	TFBC_LOSSY	63	62	---
COMPRESS_SIZE_EXT	COMPRESS_SIZE_EXT	61	61	---
PAIR_TILES	PAIR_TILES	60	60	---
X_RSRVD2	_	59	59	---
DITHER	_	58	58	---
TILERELATIVE	_	57	57	---
DOWNSCALE	_	56	56	---
SIZE_Z	SIZE	55	52	---
ROTATION	ROTATION_TYPE	51	50	---
LINESTRIDE	_	49	34	---
MEMLAYOUT	MEMLAYOUT	33	32	---
SWIZ_CHAN3	SWIZ	31	29	---
SWIZ_CHAN2	SWIZ	28	26	---
SWIZ_CHAN1	SWIZ	25	23	---
SWIZ_CHAN0	SWIZ	22	20	---
MINCLIP_X	MINCLIP	19	6	---
TWOCOMP_GAMMA	TWOCOMP_GAMMA	5	5	---
GAMMA	_	4	4	---
COMPRESSION	COMPRESSION	3	3	---
COMPRESS_SIZE	COMPRESS_SIZE	2	2	---
COMP_INDIRECT_TABLE	_	1	1	---
Y_FLIP	Y_FLIP	0	0	---

X_RSRVD2

Size 1

Not used

DITHER
Size 1

Enable dither

TILERELATIVE
Size 1

Add tile offset

DOWNSCALE
Size 1

Perform box filter downscale

LINESTRIDE
Size 16

Linestride in 2 pixel units. 0 == 2. Supports 32KDWORD stride memory write

GAMMA
Size 1

Gamma enabled

COMP_INDIRECT_TABLE
Size 1

If set indicates to the compressor that an indirect addressing is used otherwise direct addressing

---

ROGUE_CR_PBE_WORD0_MRT5
Size 64

Address: 0x00001538

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
TFBC_LOSSY	COMPRESS_SIZE_EXT	PAIR_TILES	X_RSRVD2 (_)	DITHER (_)	TILERELATIVE (_)	DOWNSCALE (_)	

55	54	53	52	51	50	49	48
SIZE_Z (SIZE)				ROTATION (ROTATION_TYPE)		LINESTRIDE (_) ...	

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)						MEMLAYOUT	

31	30	29	28	27	26	25	24
SWIZ_CHAN3 (SWIZ)			SWIZ_CHAN2 (SWIZ)			SWIZ_CHAN1 (SWIZ) ...	

23	22	21	20	19	18	17	16
SWIZ_CHAN1 (SWIZ)		SWIZ_CHAN0 (SWIZ)		MINCLIP_X (MINCLIP) ...			

15	14	13	12	11	10	9	8

MINCLIP_X (MINCLIP) ...							

7	6	5	4	3	2	1	0
MINCLIP_X (MINCLIP)		TWOCOMP_GAMMA	GAMMA (_)	COMPRESSION	COMPRESS_SIZE	COMP_INDIRECT_TABLE (_)	Y_FLIP ...

Pixel Back end State Word 0.

Name	Type	MSB	LSB	Default
TFBC_LOSSY	TFBC_LOSSY	63	62	---
COMPRESS_SIZE_EXT	COMPRESS_SIZE_EXT	61	61	---
PAIR_TILES	PAIR_TILES	60	60	---
X_RSRVD2	_	59	59	---
DITHER	_	58	58	---
TILERELATIVE	_	57	57	---
DOWNSCALE	_	56	56	---
SIZE_Z	SIZE	55	52	---
ROTATION	ROTATION_TYPE	51	50	---
LINESTRIDE	_	49	34	---
MEMLAYOUT	MEMLAYOUT	33	32	---
SWIZ_CHAN3	SWIZ	31	29	---
SWIZ_CHAN2	SWIZ	28	26	---
SWIZ_CHAN1	SWIZ	25	23	---
SWIZ_CHAN0	SWIZ	22	20	---
MINCLIP_X	MINCLIP	19	6	---
TWOCOMP_GAMMA	TWOCOMP_GAMMA	5	5	---
GAMMA	_	4	4	---
COMPRESSION	COMPRESSION	3	3	---
COMPRESS_SIZE	COMPRESS_SIZE	2	2	---
COMP_INDIRECT_TABLE	_	1	1	---
Y_FLIP	Y_FLIP	0	0	---

X_RSRVD2

Size 1

Not used

DITHER

Size 1

Enable dither

TILERELATIVE

Size 1

Add tile offset

DOWNSCALE

Size 1

Perform box filter downscale

LINESTRIDE
Size 16

Linestride in 2 pixel units. 0 == 2. Supports 32KDWORD stride memory write

GAMMA
Size 1

Gamma enabled

COMP_INDIRECT_TABLE
Size 1

If set idicates to the compressor that an indirect addressing is used otherwise direct addressing

---

ROGUE_CR_PBE_WORD0_MRT6
Size 64

Address: 0x00001540

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
TFBC_LOSSY	COMPRESS_SIZE_EXT		PAIR_TILES	X_RSRVD2 (_)	DITHER (_)	TILERELATIVE (_)	DOWNSCALE (_)

55	54	53	52	51	50	49	48
SIZE_Z (SIZE)				ROTATION (ROTATION_TYPE)		LINESTRIDE (_) ...	

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)						MEMLAYOUT	

31	30	29	28	27	26	25	24
SWIZ_CHAN3 (SWIZ)			SWIZ_CHAN2 (SWIZ)			SWIZ_CHAN1 (SWIZ) ...	

23	22	21	20	19	18	17	16
SWIZ_CHAN1 (SWIZ)			SWIZ_CHAN0 (SWIZ)			MINCLIP_X (MINCLIP) ...	

15	14	13	12	11	10	9	8
MINCLIP_X (MINCLIP) ...							

7	6	5	4	3	2	1	0
MINCLIP_X (MINCLIP)	TWOCOMP_GAMMA		GAMMA (_)	COMPRESSION	COMPRESS_SIZE	COMP_INDIRECT_TABLE (_)	Y_FLIP ...

Pixel Back end State Word 0.

Name	Type	MSB	LSB	Default
TFBC_LOSSY	TFBC_LOSSY	63	62	---
COMPRESS_SIZE_EXT	COMPRESS_SIZE_EXT	61	61	---
PAIR_TILES	PAIR_TILES	60	60	---
X_RSRVD2	_	59	59	---
DITHER	_	58	58	---

TILERELATIVE	_	57	57	---
DOWNSCALE	_	56	56	---
SIZE_Z	SIZE	55	52	---
ROTATION	ROTATION_TYPE	51	50	---
LINESTRIDE	_	49	34	---
MEMLAYOUT	MEMLAYOUT	33	32	---
SWIZ_CHAN3	SWIZ	31	29	---
SWIZ_CHAN2	SWIZ	28	26	---
SWIZ_CHAN1	SWIZ	25	23	---
SWIZ_CHAN0	SWIZ	22	20	---
MINCLIP_X	MINCLIP	19	6	---
TWOCOMP_GAMMA	TWOCOMP_GAMMA	5	5	---
GAMMA	_	4	4	---
COMPRESSION	COMPRESSION	3	3	---
COMPRESS_SIZE	COMPRESS_SIZE	2	2	---
COMP_INDIRECT_TABLE	_	1	1	---
Y_FLIP	Y_FLIP	0	0	---

X_RSRVD2
Size 1

Not used

DITHER
Size 1

Enable dither

TILERELATIVE
Size 1

Add tile offset

DOWNSCALE
Size 1

Perform box filter downscale

LINESTRIDE
Size 16

Linestride in 2 pixel units. 0 == 2. Supports 32KDWORD stride memory write

GAMMA
Size 1

Gamma enabled

COMP_INDIRECT_TABLE
Size 1

If set indicates to the compressor that an indirect addressing is used otherwise direct addressing

ROGUE_CR_PBE_WORD0_MRT7

Size 64

Address: 0x00001548

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
TFBC_LOSSY		COMPRESS_SIZE_EXT	PAIR_TILES	X_RSRVD2 (_)	DITHER (_)	TILERELATIVE (_)	DOWNSCALE (_)

55	54	53	52	51	50	49	48
SIZE_Z (SIZE)				ROTATION (ROTATION_TYPE)		LINESTRIDE (_) ...	

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)						MEMLAYOUT	

31	30	29	28	27	26	25	24
SWIZ_CHAN3 (SWIZ)			SWIZ_CHAN2 (SWIZ)			SWIZ_CHAN1 (SWIZ) ...	

23	22	21	20	19	18	17	16
SWIZ_CHAN1 (SWIZ)		SWIZ_CHAN0 (SWIZ)		MINCLIP_X (MINCLIP) ...			

15	14	13	12	11	10	9	8
MINCLIP_X (MINCLIP) ...							

7	6	5	4	3	2	1	0
MINCLIP_X (MINCLIP)		TWOCOMP_GAMMA	GAMMA (_)	COMPRESSION	COMPRESS_SIZE	COMP_INDIRECT_TABLE (_)	Y_FLIP ...

Pixel Back end State Word 0.

Name	Type	MSB	LSB	Default
TFBC_LOSSY	TFBC_LOSSY	63	62	---
COMPRESS_SIZE_EXT	COMPRESS_SIZE_EXT	61	61	---
PAIR_TILES	PAIR_TILES	60	60	---
X_RSRVD2	_	59	59	---
DITHER	_	58	58	---
TILERELATIVE	_	57	57	---
DOWNSCALE	_	56	56	---
SIZE_Z	SIZE	55	52	---
ROTATION	ROTATION_TYPE	51	50	---
LINESTRIDE	_	49	34	---
MEMLAYOUT	MEMLAYOUT	33	32	---
SWIZ_CHAN3	SWIZ	31	29	---
SWIZ_CHAN2	SWIZ	28	26	---
SWIZ_CHAN1	SWIZ	25	23	---
SWIZ_CHAN0	SWIZ	22	20	---
MINCLIP_X	MINCLIP	19	6	---
TWOCOMP_GAMMA	TWOCOMP_GAMMA	5	5	---
GAMMA	_	4	4	---

COMPRESSION	COMPRESSION	3	3	---
COMPRESS_SIZE	COMPRESS_SIZE	2	2	---
COMP_INDIRECT_TABLE	_	1	1	---
Y_FLIP	Y_FLIP	0	0	---

X_RSRVD2
Size 1

Not used

DITHER
Size 1

Enable dither

TILERELATIVE
Size 1

Add tile offset

DOWNSCALE
Size 1

Perform box filter downscale

LINESTRIDE
Size 16

Linestride in 2 pixel units. 0 == 2. Supports 32KDWORD stride memory write

GAMMA
Size 1

Gamma enabled

COMP_INDIRECT_TABLE
Size 1

If set indicates to the compressor that an indirect addressing is used otherwise direct addressing

ROGUE_CR_PBE_WORD1_MRT0
Size 64

Address: 0x00001550

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
SIZE_X (SIZE)				MINCLIP_Y (MINCLIP) ...			

55	54	53	52	51	50	49	48
MINCLIP_Y (MINCLIP) ...							

47	46	45	44	43	42	41	40
MINCLIP_Y (MINCLIP)		MAXCLIP_X (MAXCLIP) ...					

39	38	37	36	35	34	33	32
MAXCLIP_X (MAXCLIP)							

31	30	29	28	27	26	25	24
SIZE_Y (SIZE)				ZSLICE ...			

23	22	21	20	19	18	17	16
ZSLICE ...							

15	14	13	12	11	10	9	8
ZSLICE	MAXCLIP_Y (MAXCLIP) ...						

7	6	5	4	3	2	1	0
MAXCLIP_Y (MAXCLIP) ...							

Pixel Back end State Word 1.

Name	Type	MSB	LSB	Default
SIZE_X	SIZE	63	60	---
MINCLIP_Y	MINCLIP	59	46	---
MAXCLIP_X	MAXCLIP	45	32	---
SIZE_Y	SIZE	31	28	---
ZSLICE	ZSLICE	27	14	---
MAXCLIP_Y	MAXCLIP	13	0	---

ROGUE_CR_PBE_WORD1_MRT1

Size 64

Address: 0x00001558

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
SIZE_X (SIZE)				MINCLIP_Y (MINCLIP) ...			

55	54	53	52	51	50	49	48
MINCLIP_Y (MINCLIP) ...							

47	46	45	44	43	42	41	40
MINCLIP_Y (MINCLIP)		MAXCLIP_X (MAXCLIP) ...					

39	38	37	36	35	34	33	32
MAXCLIP_X (MAXCLIP)							

31	30	29	28	27	26	25	24
SIZE_Y (SIZE)				ZSLICE ...			

23	22	21	20	19	18	17	16
ZSLICE ...							

15	14	13	12	11	10	9	8
ZSLICE	MAXCLIP_Y (MAXCLIP) ...						

7	6	5	4	3	2	1	0
MAXCLIP_Y (MAXCLIP) ...							

Pixel Back end State Word 1.

Name	Type	MSB	LSB	Default
SIZE_X	SIZE	63	60	---
MINCLIP_Y	MINCLIP	59	46	---
MAXCLIP_X	MAXCLIP	45	32	---
SIZE_Y	SIZE	31	28	---
ZSLICE	ZSLICE	27	14	---
MAXCLIP_Y	MAXCLIP	13	0	---

ROGUE_CR_PBE_WORD1_MRT2

Size 64

Address: 0x00001560

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
SIZE_X (SIZE)				MINCLIP_Y (MINCLIP) ...			

55	54	53	52	51	50	49	48
MINCLIP_Y (MINCLIP) ...							

47	46	45	44	43	42	41	40
MINCLIP_Y (MINCLIP)		MAXCLIP_X (MAXCLIP) ...					

39	38	37	36	35	34	33	32
MAXCLIP_X (MAXCLIP)							

31	30	29	28	27	26	25	24
SIZE_Y (SIZE)				ZSLICE ...			

23	22	21	20	19	18	17	16
ZSLICE ...							

15	14	13	12	11	10	9	8
ZSLICE				MAXCLIP_Y (MAXCLIP) ...			

7	6	5	4	3	2	1	0
MAXCLIP_Y (MAXCLIP) ...							

Pixel Back end State Word 1.

Name	Type	MSB	LSB	Default
SIZE_X	SIZE	63	60	---
MINCLIP_Y	MINCLIP	59	46	---
MAXCLIP_X	MAXCLIP	45	32	---
SIZE_Y	SIZE	31	28	---
ZSLICE	ZSLICE	27	14	---
MAXCLIP_Y	MAXCLIP	13	0	---

ROGUE_CR_PBE_WORD1_MRT3

Size 64

Address: 0x00001568

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
SIZE_X (SIZE)				MINCLIP_Y (MINCLIP) ...			

55	54	53	52	51	50	49	48
MINCLIP_Y (MINCLIP) ...							

47	46	45	44	43	42	41	40
MINCLIP_Y (MINCLIP)		MAXCLIP_X (MAXCLIP) ...					

39	38	37	36	35	34	33	32
MAXCLIP_X (MAXCLIP)							

31	30	29	28	27	26	25	24
SIZE_Y (SIZE)				ZSLICE ...			

23	22	21	20	19	18	17	16
ZSLICE ...							

15	14	13	12	11	10	9	8
ZSLICE	MAXCLIP_Y (MAXCLIP) ...						

7	6	5	4	3	2	1	0
MAXCLIP_Y (MAXCLIP) ...							

Pixel Back end State Word 1.

Name	Type	MSB	LSB	Default
SIZE_X	SIZE	63	60	---
MINCLIP_Y	MINCLIP	59	46	---
MAXCLIP_X	MAXCLIP	45	32	---
SIZE_Y	SIZE	31	28	---
ZSLICE	ZSLICE	27	14	---
MAXCLIP_Y	MAXCLIP	13	0	---

ROGUE_CR_PBE_WORD1_MRT4

Size 64

Address: 0x00001570

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
SIZE_X (SIZE)				MINCLIP_Y (MINCLIP) ...			

55	54	53	52	51	50	49	48
MINCLIP_Y (MINCLIP) ...							

47	46	45	44	43	42	41	40
MINCLIP_Y (MINCLIP)		MAXCLIP_X (MAXCLIP) ...					

39	38	37	36	35	34	33	32
MAXCLIP_X (MAXCLIP)							

31	30	29	28	27	26	25	24
SIZE_Y (SIZE)				ZSLICE ...			

23	22	21	20	19	18	17	16
ZSLICE ...							

15	14	13	12	11	10	9	8
ZSLICE				MAXCLIP_Y (MAXCLIP) ...			

7	6	5	4	3	2	1	0
MAXCLIP_Y (MAXCLIP) ...							

Pixel Back end State Word 1.

Name	Type	MSB	LSB	Default
SIZE_X	SIZE	63	60	---
MINCLIP_Y	MINCLIP	59	46	---
MAXCLIP_X	MAXCLIP	45	32	---
SIZE_Y	SIZE	31	28	---
ZSLICE	ZSLICE	27	14	---
MAXCLIP_Y	MAXCLIP	13	0	---

ROGUE_CR_PBE_WORD1_MRT5

Size 64

Address: 0x00001578

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
SIZE_X (SIZE)				MINCLIP_Y (MINCLIP) ...			

55	54	53	52	51	50	49	48
MINCLIP_Y (MINCLIP) ...							

47	46	45	44	43	42	41	40
MINCLIP_Y (MINCLIP)		MAXCLIP_X (MAXCLIP) ...					

39	38	37	36	35	34	33	32
MAXCLIP_X (MAXCLIP)							

31	30	29	28	27	26	25	24
SIZE_Y (SIZE)				ZSLICE ...			

23	22	21	20	19	18	17	16
ZSLICE ...							

15	14	13	12	11	10	9	8

ZSLICE	MAXCLIP_Y (MAXCLIP) ...

7	6	5	4	3	2	1	0
MAXCLIP_Y (MAXCLIP) ...							

Pixel Back end State Word 1.

Name	Type	MSB	LSB	Default
SIZE_X	SIZE	63	60	---
MINCLIP_Y	MINCLIP	59	46	---
MAXCLIP_X	MAXCLIP	45	32	---
SIZE_Y	SIZE	31	28	---
ZSLICE	ZSLICE	27	14	---
MAXCLIP_Y	MAXCLIP	13	0	---

ROGUE_CR_PBE_WORD1_MRT6

Size 64

Address: 0x00001580

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
SIZE_X (SIZE)				MINCLIP_Y (MINCLIP) ...			

55	54	53	52	51	50	49	48
MINCLIP_Y (MINCLIP) ...							

47	46	45	44	43	42	41	40
MINCLIP_Y (MINCLIP)		MAXCLIP_X (MAXCLIP) ...					

39	38	37	36	35	34	33	32
MAXCLIP_X (MAXCLIP)							

31	30	29	28	27	26	25	24
SIZE_Y (SIZE)				ZSLICE ...			

23	22	21	20	19	18	17	16
ZSLICE ...							

15	14	13	12	11	10	9	8
ZSLICE	MAXCLIP_Y (MAXCLIP) ...						

7	6	5	4	3	2	1	0
MAXCLIP_Y (MAXCLIP) ...							

Pixel Back end State Word 1.

Name	Type	MSB	LSB	Default
SIZE_X	SIZE	63	60	---
MINCLIP_Y	MINCLIP	59	46	---
MAXCLIP_X	MAXCLIP	45	32	---
SIZE_Y	SIZE	31	28	---
ZSLICE	ZSLICE	27	14	---

MAXCLIP_Y	MAXCLIP	13	0	---

ROGUE_CR_PBE_WORD1_MRT7

Size 64

Address: 0x00001588

Access: read-write

Member of groups: pbe texas

63	62	61	60	59	58	57	56
SIZE_X (SIZE)				MINCLIP_Y (MINCLIP) ...			

55	54	53	52	51	50	49	48
MINCLIP_Y (MINCLIP) ...							

47	46	45	44	43	42	41	40
MINCLIP_Y (MINCLIP)		MAXCLIP_X (MAXCLIP) ...					

39	38	37	36	35	34	33	32
MAXCLIP_X (MAXCLIP)							

31	30	29	28	27	26	25	24
SIZE_Y (SIZE)				ZSLICE ...			

23	22	21	20	19	18	17	16
ZSLICE ...							

15	14	13	12	11	10	9	8
ZSLICE				MAXCLIP_Y (MAXCLIP) ...			

7	6	5	4	3	2	1	0
MAXCLIP_Y (MAXCLIP) ...							

Pixel Back end State Word 1.

Name	Type	MSB	LSB	Default
SIZE_X	SIZE	63	60	---
MINCLIP_Y	MINCLIP	59	46	---
MAXCLIP_X	MAXCLIP	45	32	---
SIZE_Y	SIZE	31	28	---
ZSLICE	ZSLICE	27	14	---
MAXCLIP_Y	MAXCLIP	13	0	---

ROGUE_CR_PBE_WORD2_MRT0

Size 64

Address: 0x00001580

Access: read-write

Direction: both**SCOPE:** 3D

Member of groups: pbe_shared

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)							

31	30	29	28	27	26	25	24
SW_BYTEMASK ...							

23	22	21	20	19	18	17	16
SW_BYTEMASK ...							

15	14	13	12	11	10	9	8
SW_BYTEMASK ...							

7	6	5	4	3	2	1	0
SW_BYTEMASK ...							

MRT Word 2 - Defined by ROGUE_CR_PBE_STATE2

Name	MSB	LSB	Default
LINESTRIDE	47	32	---
SW_BYTEMASK	31	0	---

LINESTRIDE

Size 16

Linestride in 1 pixel units. Up to 64k pixels (HW Currently limited to 16k), this is used for Linear textures and twiddle textures with FBC

ROGUE_CR_PBE_WORD2_MRT1

Size 64

Address: 0x00001588

Access: read-write

Direction: both**SCOPE:** 3D

Member of groups: pbe_shared

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)							

31	30	29	28	27	26	25	24
SW_BYTEMASK ...							

23	22	21	20	19	18	17	16
SW_BYTEMASK ...							

15	14	13	12	11	10	9	8
SW_BYTEMASK ...							

7	6	5	4	3	2	1	0
SW_BYTEMASK ...							

MRT Word 2 - Defined by ROGUE_CR_PBE_STATE2

Name	MSB	LSB	Default
LINESTRIDE	47	32	---
SW_BYTEMASK	31	0	---

LINESTRIDE

Size 16

Linestride in 1 pixel units. Up to 64k pixels (HW Currently limited to 16k), this is used for Linear textures and twiddle textures with FBC

ROGUE_CR_PBE_WORD2_MRT2

Size 64

Address: 0x00001590

Access: read-write

Direction: both**SCOPE:** 3D

Member of groups: pbe_shared

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)							

31	30	29	28	27	26	25	24
SW_BYTEMASK ...							

23	22	21	20	19	18	17	16
SW_BYTEMASK ...							

15	14	13	12	11	10	9	8
SW_BYTEMASK ...							

7	6	5	4	3	2	1	0
SW_BYTEMASK ...							

MRT Word 2 - Defined by ROGUE_CR_PBE_STATE2

Name	MSB	LSB	Default

LINESTRIDE	47	32	---
SW_BYTEMASK	31	0	---

LINESTRIDE

Size 16

Linestride in 1 pixel units. Up to 64k pixels (HW Currently limited to 16k), this is used for Linear textures and twiddle textures with FBC

ROGUE_CR_PBE_WORD2_MRT3

Size 64

Address: 0x00001598

Access: read-write

Direction: both**SCOPE:** 3D

Member of groups: pbe_shared

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)							

31	30	29	28	27	26	25	24
SW_BYTEMASK ...							

23	22	21	20	19	18	17	16
SW_BYTEMASK ...							

15	14	13	12	11	10	9	8
SW_BYTEMASK ...							

7	6	5	4	3	2	1	0
SW_BYTEMASK ...							

MRT Word 2 - Defined by ROGUE_CR_PBE_STATE2

Name	MSB	LSB	Default
LINESTRIDE	47	32	---
SW_BYTEMASK	31	0	---

LINESTRIDE

Size 16

Linestride in 1 pixel units. Up to 64k pixels (HW Currently limited to 16k), this is used for Linear textures and twiddle textures with FBC

ROGUE_CR_PBE_WORD2_MRT4

Size 64

Address: 0x000015a0

Access: read-write

Direction: both**SCOPE:** 3D

Member of groups: pbe_shared

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)							

31	30	29	28	27	26	25	24
SW_BYTEMASK ...							

23	22	21	20	19	18	17	16
SW_BYTEMASK ...							

15	14	13	12	11	10	9	8
SW_BYTEMASK ...							

7	6	5	4	3	2	1	0
SW_BYTEMASK ...							

MRT Word 2 - Defined by ROGUE_CR_PBE_STATE2

Name	MSB	LSB	Default
LINESTRIDE	47	32	---
SW_BYTEMASK	31	0	---

LINESTRIDE

Size 16

Linestride in 1 pixel units. Up to 64k pixels (HW Currently limited to 16k), this is used for Linear textures and twiddle textures with FBC

ROGUE_CR_PBE_WORD2_MRT5

Size 64

Address: 0x000015a8

Access: read-write

Direction: both**SCOPE:** 3D

Member of groups: pbe_shared

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)							

31	30	29	28	27	26	25	24
SW_BYTEMASK ...							

23	22	21	20	19	18	17	16
SW_BYTEMASK ...							

15	14	13	12	11	10	9	8
SW_BYTEMASK ...							

7	6	5	4	3	2	1	0
SW_BYTEMASK ...							

MRT Word 2 - Defined by ROGUE_CR_PBE_STATE2

Name	MSB	LSB	Default
LINESTRIDE	47	32	---
SW_BYTEMASK	31	0	---

LINESTRIDE

Size 16

Linestride in 1 pixel units. Up to 64k pixels (HW Currently limited to 16k), this is used for Linear textures and twiddle textures with FBC

ROGUE_CR_PBE_WORD2_MRT6

Size 64

Address: 0x000015b0

Access: read-write

Direction: both**SCOPE:** 3D

Member of groups: pbe_shared

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)							

31	30	29	28	27	26	25	24
SW_BYTEMASK ...							

23	22	21	20	19	18	17	16
SW_BYTEMASK ...							

15	14	13	12	11	10	9	8
SW_BYTEMASK ...							

7	6	5	4	3	2	1	0
SW_BYTEMASK ...							

MRT Word 2 - Defined by ROGUE_CR_PBE_STATE2

Name	MSB	LSB	Default
LINESTRIDE	47	32	---
SW_BYTEMASK	31	0	---

LINESTRIDE

Size 16

Linestride in 1 pixel units. Up to 64k pixels (HW Currently limited to 16k), this is used for Linear textures and twiddle textures with FBC

ROGUE_CR_PBE_WORD2_MRT7

Size 64

Address: 0x000015b8

Access: read-write

Direction: both**SCOPE:** 3D

Member of groups: pbe_shared

63	62	61	60	59	58	57	56
reserved							

55	54	53	52	51	50	49	48
reserved							

47	46	45	44	43	42	41	40
LINESTRIDE (_) ...							

39	38	37	36	35	34	33	32
LINESTRIDE (_)							

31	30	29	28	27	26	25	24
SW_BYTEMASK ...							

23	22	21	20	19	18	17	16
SW_BYTEMASK ...							

15	14	13	12	11	10	9	8
SW_BYTEMASK ...							

7	6	5	4	3	2	1	0
SW_BYTEMASK ...							

MRT Word 2 - Defined by ROGUE_CR_PBE_STATE2

Name	MSB	LSB	Default
LINESTRIDE	47	32	---
SW_BYTEMASK	31	0	---

LINESTRIDE

Size 16

Linestride in 1 pixel units. Up to 64k pixels (HW Currently limited to 16k), this is used for Linear textures and twiddle textures with FBC

ROGUE_CR_PDS_BGRND0_BASE

Size 64

Address: 0x000006a0

Access: read-write

Member of groups: texas3 texas hub

63	62	61	60	59	58	57	56
TEXUNICODE_ADDR (PDS_ADDR) ...							

55	54	53	52	51	50	49	48
TEXUNICODE_ADDR (PDS_ADDR) ...							

47	46	45	44	43	42	41	40
TEXUNICODE_ADDR (PDS_ADDR) ...							

39	38	37	36	35	34	33	32
TEXUNICODE_ADDR (PDS_ADDR)				*reserved*			

31	30	29	28	27	26	25	24
SHADER_ADDR (PDS_ADDR) ...							

23	22	21	20	19	18	17	16
SHADER_ADDR (PDS_ADDR) ...							

15	14	13	12	11	10	9	8
SHADER_ADDR (PDS_ADDR) ...							

7	6	5	4	3	2	1	0
				reserved			

PDS Background Setup Word 0

Name	Type	MSB	LSB	Default
TEXUNICODE_ADDR	PDS_ADDR	63	36	---
SHADER_ADDR	PDS_ADDR	31	4	---

ROGUE_CR_PDS_BGRND1_BASE

Size 64

Address: 0x000006a8

Access: read-write

Member of groups: texas3 texas hub

63	62	61	60	59	58	57	56
TEXTUREDATA_ADDR (PDS_ADDR) ...							

55	54	53	52	51	50	49	48
TEXTUREDATA_ADDR (PDS_ADDR) ...							

47	46	45	44	43	42	41	40
TEXTUREDATA_ADDR (PDS_ADDR) ...							

39	38	37	36	35	34	33	32
TEXTUREDATA_ADDR (PDS_ADDR)				*reserved*			

31	30	29	28	27	26	25	24
VARYING_ADDR (PDS_ADDR) ...							

23	22	21	20	19	18	17	16
VARYING_ADDR (PDS_ADDR) ...							

15	14	13	12	11	10	9	8
VARYING_ADDR (PDS_ADDR) ...							

7	6	5	4	3	2	1	0
VARYING_ADDR (PDS_ADDR)				*reserved*			

PDS Background Setup Word 1

Name	Type	MSB	LSB	Default
TEXTUREDATA_ADDR	PDS_ADDR	63	36	---
VARYING_ADDR	PDS_ADDR	31	4	---

ROGUE_CR_PDS_BGRND3_SIZEINFO

Size 64

Address: 0x000006b8

Access: read-write

Member of groups: texas3 texas hub

63	62	61	60	59	58	57	56
USC_SHAREDSIZE (_) ...							

55	54	53	52	51	50	49	48
USC_SHAREDSIZE (_)	*reserved*						

47	46	45	44	43	42	41	40
reserved	PDS_BATCHNUM (_) ...						

39	38	37	36	35	34	33	32
PDS_BATCHNUM (_)							

31	30	29	28	27	26	25	24
PDS_UNIFORMSIZE (_) ...							

23	22	21	20	19	18	17	16
PDS_UNIFORMSIZE (_)	PDS_TEXTURESTATESIZE (_)						

15	14	13	12	11	10	9	8
PDS_VARYINGSIZE (_)						USC_VARYINGSIZE (_) ...	

7	6	5	4	3	2	1	0
USC_VARYINGSIZE (_)	PDS_TEMPSIZE (_) ...						

If any of the size fields are 0, then that program will not be run. PDS_BGRND_PIXELSHADERSIZE is always 2 128 Bit Words

Name	Type	MSB	LSB	Default
USC_SHAREDSIZE	_	63	55	---
PDS_BATCHNUM	_	45	32	---
PDS_UNIFORMSIZE	_	31	23	---
PDS_TEXTURESTATESIZE	_	22	16	---
PDS_VARYINGSIZE	_	15	10	---
USC_VARYINGSIZE	_	9	4	---
PDS_TEMPSIZE	_	3	0	---

USC_SHAREDSIZE
Size 9

The common store allocation size for the shared registers (texture and uniform data commbined)

PDS_BATCHNUM
Size 14

The batch ID to be associated with the background

PDS_UNIFORMSIZE
Size 9

The size of the Uniform PDS Data Segment in 128 bit words

PDS_TEXTURESTATESIZE
Size 7

The size of the Texture PDS Data Segment in 128 bit words

PDS_VARYINGSIZE
Size 6

The size of the Varying/Coefficient PDS Data Segment in 128 bit words

USC_VARYINGSIZE
Size 6

The size of the Varying/Coefficient USC Common Store Data in 4x128 bit words

PDS_TEMPSIZE
Size 4

0 = 0 128 bit words, 1 = 1 128 bit word, this applies to coefficient, uniform and varying state

---

ROGUE_CR_PDS_COEFF_FREE_PROG
Size 62

Address: 0x00000778

Access: read-write

Member of groups: blackpearl

63	62	61	60	59	58	57	56

-	DATA_SIZE (_)

55	54	53	52	51	50	49	48
DATA_ADDR (_) ...							

47	46	45	44	43	42	41	40
DATA_ADDR (_) ...							

39	38	37	36	35	34	33	32
DATA_ADDR (_) ...							

31	30	29	28	27	26	25	24
DATA_ADDR (_)				CODE_ADDR (_) ...			

23	22	21	20	19	18	17	16
CODE_ADDR (_) ...							

15	14	13	12	11	10	9	8
CODE_ADDR (_) ...							

7	6	5	4	3	2	1	0
CODE_ADDR (_) ...							

The PDS code address for the PDS coefficient free program to free any zombie coefficient resource allocated by the HS shader. This program has a zero size of the following resource: temp, unified store, common store, usv store. The data size is 256bits by default. This pds programm will spawn a dummy usc shader as well

Name	MSB	LSB	Default
DATA_SIZE	61	56	0x2
DATA_ADDR	55	28	---
CODE_ADDR	27	0	---

ROGUE_CR_PDS_CTRL

Size 63

Address: 0x00000600

Access: read-write

Member of groups: texas3 texas hub

63	62	61	60	59	58	57	56
-	*reserved*						

55	54	53	52	51	50	49	48
SM_OVERLAP_ENABLE (_)	*reserved*						

47	46	45	44	43	42	41	40
reserved							

39	38	37	36	35	34	33	32
reserved							

31	30	29	28	27	26	25	24
MAX_NUM_CDM_TASKS (_)							

23	22	21	20	19	18	17	16

MAX_NUM_PDM_TASKS (_)

15	14	13	12	11	10	9	8
MAX_NUM_VDM_TASKS (_)							

7	6	5	4	3	2	1	0
reserved							

Controls the maximum number of tasks per data master (per USC). There are a maximum of 48 tasks in the system

Name	Type	MSB	LSB	Default
SM_OVERLAP_ENABLE	_	55	55	0x1
MAX_NUM_CDM_TASKS	_	31	24	0x30
MAX_NUM_PDM_TASKS	_	23	16	0x30
MAX_NUM_VDM_TASKS	_	15	8	0x30

MAX_NUM_VDM_TASKS

Size 8

The maximum number of vertex tasks (VS, HS, GS when Tess not enabled) allowed on each USC, range 0 to 39 (Note reduced range to prevent Pixel /VDM system deadlock)

MAX_NUM_PDM_TASKS

Size 8

The maximum number of pixel tasks allowed on each USC, range 0 to 48

MAX_NUM_CDM_TASKS

Size 8

The maximum number of compute tasks allowed on each USC, range 0 to 48

SM_OVERLAP_ENABLE

Size 1

Enable per Data Master slot tracking within the PDS Slot Manager (SM) for improved performance while running overlapped

ROGUE_CR_PM_DEALLOCATED_MASK_STATUS

Size 20

Address: 0x00000360

Access: readonly

Member of groups: jones tornado bifpmcache

23	22	21	20	19	18	17	16
-				*reserved*			

15	14	13	12	11	10	9	8
TOP (_) ...							

7	6	5	4	3	2	1	0
TOP (_) ...							

Name	Type	MSB	LSB	Default
TOP	_	15	0	---

TOP
Size 16

This status register contains a bitmask of the macrotiles freed at this point in the render

ROGUE_CR_PM_PDS_MTILEFREE_STATUS">

ROGUE_CR_PM_PDS_MTILEFREE_STATUS
Size 17

Address: 0x00000370

Access: readonly

Member of groups: jones tornado bifpmcache

23	22	21	20	19	18	17	16
-							OP (_) ...

15	14	13	12	11	10	9	8
OP (_) ...							

7	6	5	4	3	2	1	0
OP (_) ...							

Name	Type	MSB	LSB	Default
OP	_	16	0	---

OP
Size 17

This status register indicates the macrotile number of the PDSs current macrotile free request

ROGUE_CR_PPP_CTRL
Size 13

Address: 0x00000c88

Access: read-write

Member of groups: jones blackpearl tiling ta

15	14	13	12	11	10	9	8
-			VPT_SCISSOR (_)	FLUSH_MODE (_)	BFCULL_RESTRICT_CLIP (_)	FIXED_POINT_FORMAT (_)	DEFAULT_POINT_SIZE (_)

7	6	5	4	3	2	1	0
BFCULL1_DISABLE (_)	BFCULL2_DISABLE (_)	FCCULL_DISABLE (_)	OSCULL_DISABLE (_)	PSOCULL_DISABLE (_)	SOCULL_DISABLE (_)	WCLAMPEN (_)	OPENGL (_) ...

This register controls the global setup of the PPP.

Name	Type	MSB	LSB	Default
VPT_SCISSOR	_	12	12	0
FLUSH_MODE	_	11	11	0
BFCULL_RESTRICT_CLIP	_	10	10	---
FIXED_POINT_FORMAT	_	9	9	---
DEFAULT_POINT_SIZE	_	8	8	---
BFCULL1_DISABLE	_	7	7	---

BFCULL2_DISABLE	_	6	6	---
FCCULL_DISABLE	_	5	5	---
OSCULL_DISABLE	_	4	4	---
PSOCULL_DISABLE	_	3	3	---
SOCULL_DISABLE	_	2	2	---
WCLAMPEN	_	1	1	---
OPENGL	_	0	0	---

VPT_SCISSOR
Size 1

When 0 the PPP will insert state updates on change of VPT ID, When 1 this feature is disabled

FLUSH_MODE
Size 1

when 0 PPP will supress end of draw call flushed from reaching the Clipper and TA pipeline, This will break batch number funstionality but will give better primitive block utiliastion. when 1 PPP will not supress any flushes

BFCULL_RESTRICT_CLIP
Size 1

When set, clipped primitives are only back-face culled after the clipper. 0 Enable early back face cull for clipped primitives 1 Disable early cull

FIXED_POINT_FORMAT
Size 1

When set, the PPP will use a fixed point format of 16.8 rather than 16.4. 0 16.4 fixed point format 1 16.8 fixed point format

DEFAULT_POINT_SIZE
Size 1

When set, the PPP will use the default point size rather than reading it from the vertex. 0 Point size read from vertex 1 Default point size of 3F800000 used

BFCULL1_DISABLE
Size 1

Disable for fully clipped culling 0 First back face cull block enabled 1 First back face cull block disabled

BFCULL2_DISABLE
Size 1

Disable for fully clipped culling 0 Second back face cull block enabled 1 Second back face cull block disabled

FCCULL_DISABLE
Size 1

Disable for fully clipped culling 0 Fully clipped culling enabled 1 Fully clipped culling disabled

OSCULL_DISABLE
Size 1

Disable for off screen culling 0 Off screen culling enabled 1 Off screen culling disabled

PSOCULL_DISABLE
Size 1

Disable for perfect small object culling 0 Perfect small object culling enabled 1 Perfect small object culling disabled

SOCULL_DISABLE
Size 1

Disable for small object culling 0 Small object culling enabled 1 Small object culling disabled

WCLAMPEN
Size 1

Enable W clamping 0 W clamping disabled 1 W clamping enabled

OPENGL
Size 1

Select OpenGL or D3D mode 0 D3D 1 OpenGL

ROGUE_CR_TA_CONTEXT_STATE_BASE
Size 40

Address: 0x00000cc0

Access: read-write

Member of groups: blackpearl jones tornado ta hub

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)				*reserved*			

The base address in external memory of the TA's context state buffer, to which the PPP will store the state on a context store and from which the VDM will reload on a context resume

Name	Type	MSB	LSB	Default
ADDR	_	39	4	---

ADDR
Size 36

1TB range, 128-bit aligned base address

ROGUE_CR_TDM_CB
Size: 20

Address: 0x00002610**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** 2D

Register banks: tdm_dv jones

Kick pipeline: two_d_fe

23	22	21	20	19	18	17	16
-				SIZE (_) ...			

15	14	13	12	11	10	9	8
SIZE (_) ...							

7	6	5	4	3	2	1	0
SIZE (_)				*reserved*			

TDM Circular Buffer Size in 256-bit words

Name	MSB	LSB	Default	Description	Bank Filter
SIZE	19	5	0	1MB range, 256-bit granular TDM Circular Buffer Size	

ROGUE_CR_TDM_CB.SIZE

Size: 15

Type: Define

ALIGN: 5

1MB range, 256-bit granular TDM Circular Buffer Size

ROGUE_CR_TDM_CB_BASE

Size: 40

Address: 0x00002608**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** 2D

Register banks: tdm_dv jones

Kick pipeline: two_d_fe

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_)				*reserved*			

7	6	5	4	3	2	1	0
reserved							

TDM Circular Buffer base adddress

Name	MSB	LSB	Default	Description	Bank Filter
ADDR	39	12	0	1 TB range, 4KB aligned base address for TDM control stream circular buffer	

ROGUE_CR_TDM_CB_BASE.ADDR

Size: 28

Type: Define

ALIGN: 12

1 TB range, 4KB aligned base address for TDM control stream circular buffer

ROGUE_CR_TDM_CB_QUEUE

Size: 40

Address: 0x00002618**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** 2D

Register banks: tdm_dv jones

Kick pipeline: two_d_fe

39	38	37	36	35	34	33	32
CTRL_BASE_ADDR (_) ...							

31	30	29	28	27	26	25	24
CTRL_BASE_ADDR (_) ...							

23	22	21	20	19	18	17	16
CTRL_BASE_ADDR (_) ...							

15	14	13	12	11	10	9	8
CTRL_BASE_ADDR (_) ...							

7	6	5	4	3	2	1	0
CTRL_BASE_ADDR (_)	*reserved*						

TDM Circular Buffer Queue Control Base Address

Name	MSB	LSB	Default	Description	Bank Filter
CTRL_BASE_ADDR	39	7	0	1 TB range, 1024-bit aligned base address for TDM queue control structure	

ROGUE_CR_TDM_CB_QUEUE.CTRL_BASE_ADDR

Size: 33

Type: Define

ALIGN: 7

ROGUE_CR_TDM_CONTEXT_STATE_BASE

Size: 40

Address: 0x00002648**Default:** 0

Type: Register**Direction**: read-write**SCOPE:** 2D

Register banks: tdm_dv jones

Kick pipeline: two_d_fe

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)	*reserved*						

The base address in external memory of the TDM's context state buffer, to which it will store its snapshot state on a context store and from which it will reload on a TDM start pulse.

Name	MSB	LSB	Default	Description	Bank Filter
ADDR	39	7	0	1TB range, 1024-bit aligned base address	

ROGUE_CR_TDM_CONTEXT_STATE_BASE.ADDR

Size: 33

Type: Define

ALIGN: 7

1TB range, 1024-bit aligned base address

ROGUE_CR_TE_PSG

Size 23

Address: 0x00000c28

Access: read-write

Member of groups: jones tiling tornado ta

23	22	21	20	19	18	17	16
-	FORCE_PROTECT (_)	CS_SIZE (_)	ENABLE_PWR_GATE_STATE (_)	ENABLE_CONTEXT_STATE_RESTORE (_)	ZONLYRENDER (_)	COMPLETEONTERMINATE (_)	*reserved*

15	14	13	12	11	10	9	8
reserved	CACHE_BYPASS (_)	FORCENEWSTATE (_)	*reserved*	REGION_STRIDE (_) ...			

7	6	5	4	3	2	1	0
REGION_STRIDE (_) ...							

This register defines the global control for the Parameter Stream Generator within the Tiling Co-Processor. This module formats the display list generated by the Tiling Co-Processor.

Name	Type	MSB	LSB	Default
FORCE_PROTECT	_	22	22	0
CS_SIZE	_	21	21	0
ENABLE_PWR_GATE_STATE	_	20	20	0x1
ENABLE_CONTEXT_STATE_RESTORE	_	19	19	0
ZONLYRENDER	_	18	18	0
COMPLETEONTERMINATE	_	17	17	0x1
CACHE_BYPASS	_	14	14	0
FORCENEWSTATE	_	13	13	0
REGION_STRIDE	_	10	0	0x6

FORCE_PROTECT
Size 1

When set, the TE shall force the PROTECT bit to 1 for all tiles

CS_SIZE
Size 1

Size of control stream chunk. 0x0 512 bit 0x1 1024 bit

ENABLE_PWR_GATE_STATE
Size 1

Enables TE PSG power gate state init. 0x0 Disable 0x1 Enable

ENABLE_CONTEXT_STATE_RESTORE
Size 1

Enables sampling of Driver TE_STATE_ISP_STATE_ID and TE_ACTIVE_MTILE registers on context switch/restore when set, when reset current local value is preserved.

ZONLYRENDER
Size 1

Don't invalidate Tail Pointer Cache entries on a Terminate command. Only effective when COMPLETEONTERMINATE is 0x0 0x0 Do Invalidate 0x1 Don't Invalidate

COMPLETEONTERMINATE
Size 1

0x1 Write region headers, terminate streams and invalidate tail pointer cache entries on terminate. 0x0 If ZONLYRENDER = 0x0 then force an Interrupt, however if ZONLYRENDER = 0x1 then write region headers and terminate streams.

CACHE_BYPASS
Size 1

when set, PSG sets its write only cache to bypass mode, effectively disabling the cache

FORCENEWSTATE
Size 1

Always embed state information in control stream. Debug only.

REGION_STRIDE
Size 11

Number of 4kB Pages devoted to region headers for each Render Target - max needed = 0x500

ROGUE_CR_TE_PSGREGION_ADDR
Size 40

Address: 0x00000c38

Access: read-write

Member of groups: jones tiling tornado ta

39	38	37	36	35	34	33	32

HEAP (_)	BASE (_) ...

31	30	29	28	27	26	25	24
BASE (_) ...							

23	22	21	20	19	18	17	16
BASE (_) ...							

15	14	13	12	11	10	9	8
BASE (_) ...							

7	6	5	4	3	2	1	0
BASE (_)	*reserved*						

This register defines the base address in memory of the Region Header writes by the TA. Region headers are the first part of the display list and contain an entry per tile with information on global setup and a link address to parameters.

Name	Type	MSB	LSB	Default
HEAP	_	39	34	---
BASE	_	33	6	---

HEAP

Size 6

1TB Addressable, 16GB aligned Heap Address for Region Header writes

BASE

Size 28

16GB Addressable, 512-bit aligned Base Address for Region Header writes

---

ROGUE_CR_TLA_CMD_STREAM

Size 50

Address: 0x00000188

Access: read-write

Member of groups: jones sidekick2 sidekick

55	54	53	52	51	50	49	48
-						BURST_SIZE (_) ...	

47	46	45	44	43	42	41	40
BURST_SIZE (_)							

39	38	37	36	35	34	33	32
ADDRESS (_) ...							

31	30	29	28	27	26	25	24
ADDRESS (_) ...							

23	22	21	20	19	18	17	16
ADDRESS (_) ...							

15	14	13	12	11	10	9	8
ADDRESS (_) ...							

7	6	5	4	3	2	1	0
ADDRESS (_) ...							

TLA command stream location (address) and size.

Name	MSB	LSB	Default
BURST_SIZE	49	40	0
ADDRESS	39	0	0

BURST_SIZE

Size 10

Represents the number of 64-bit commands to fetch

ADDRESS

Size 40

Address the TLA should start fetching command stream data from. Minimum granularity is 64-bit aligned

---

ROGUE_CR_TPU

Size 9

Address: 0x00001780

Access: read-write

Member of groups: usc tpu tpu_mcu_l0

15	14	13	12	11	10	9	8
-							MCU_PDS_L0_OFF (_)

7	6	5	4	3	2	1	0
TAG_CEM_64_FACE_PACKING (_)	TAG_ENABLE_MMU_PREFETCH (_)	TAG_CEM_4K_FACE_PACKING (_)	MADD_CONFIG_L0OFF (_)	TAG_CEM_FACE_PACKING (_)	TAG_CEMEDGE_DONTFILTER (_)	TAG_CEMGRAD_DONTNEGATE (_)	MADD_CONFIG_DXT35_TRANSOVR (_) ...

Global control to TPU_MCU_L0|tpu

Name	Type	MSB	LSB	Default
MCU_PDS_L0_OFF	_	8	8	0
TAG_CEM_64_FACE_PACKING	_	7	7	0
TAG_ENABLE_MMU_PREFETCH	_	6	6	0x1
TAG_CEM_4K_FACE_PACKING	_	5	5	0
MADD_CONFIG_L0OFF	_	4	4	0
TAG_CEM_FACE_PACKING	_	3	3	0
TAG_CEMEDGE_DONTFILTER	_	2	2	0
TAG_CEMGRAD_DONTNEGATE	_	1	1	0
MADD_CONFIG_DXT35_TRANSOVR	_	0	0	0

MADD_CONFIG_DXT35_TRANSOVR

Size 1

When set this disables alternative mode implied by colour0 > colour1 for DXT3 to DXT5

TAG_CEMGRAD_DONTNEGATE

Size 1

Pixel data master. Disable negation for user supplied gradients for cem swap i.e. will only swap dudx etc not negate

TAG_CEMEDGE_DONTFILTER
Size 1

Pixel data master. Disable filtering over edges/corners for CEM. When set to 1, HW will be seemfull, ie, always stay in the current map, always honour the addressmode. When set to 0, HW will be seemless, ie, ignore addressmode, filter between faces at the edges/corners

TAG_CEM_FACE_PACKING
Size 1

Pixel data master. Enable dword alignment between CEM faces when set to 1

MADD_CONFIG_L0OFF
Size 1

When set this disables MADD P0 L0 cache

TAG_CEM_4K_FACE_PACKING
Size 1

Pixel data master. Enable 4K-byte alignment between CEM faces when set to 1. It applies for both when mipmap is enabled or disabled

TAG_ENABLE_MMU_PREFETCH
Size 1

Enables generation of prefetch requests to the MMU

TAG_CEM_64_FACE_PACKING
Size 1

Pixel data master. Enable 64-byte alignment between CEM faces when set to 1. It applies for both when mipmap is enabled or disabled

MCU_PDS_L0_OFF
Size 1

Turn off MCU PDSL0 cache

ROGUE_CR_TPU_BORDER_COLOUR_TABLE_CDM
Size 38

Address: 0x000017a8

Access: read-write

Member of groups: tpu tpu_mcu_l0

39	38	37	36	35	34	33	32
-	BORDER_COLOUR_TABLE_ADDRESS (_) ...						

31	30	29	28	27	26	25	24
BORDER_COLOUR_TABLE_ADDRESS (_) ...							

23	22	21	20	19	18	17	16
BORDER_COLOUR_TABLE_ADDRESS (_) ...							

15	14	13	12	11	10	9	8
BORDER_COLOUR_TABLE_ADDRESS (_) ...							

7	6	5	4	3	2	1	0
BORDER_COLOUR_TABLE_ADDRESS (_) ...							

Base address for the border colour table

Name	Type	MSB	LSB	Default
BORDER_COLOUR_TABLE_ADDRESS	_	37	0	0

BORDER_COLOUR_TABLE_ADDRESS

Size 38

Base address DWORD aligned for the location in memory of the border colour table for the CDM

ROGUE_CR_TPU_BORDER_COLOUR_TABLE_PDM

Size 38

Address: 0x00001790

Access: read-write

Member of groups: tpu tpu_mcu_l0

39	38	37	36	35	34	33	32
-	BORDER_COLOUR_TABLE_ADDRESS (_) ...						

31	30	29	28	27	26	25	24
BORDER_COLOUR_TABLE_ADDRESS (_) ...							

23	22	21	20	19	18	17	16
BORDER_COLOUR_TABLE_ADDRESS (_) ...							

15	14	13	12	11	10	9	8
BORDER_COLOUR_TABLE_ADDRESS (_) ...							

7	6	5	4	3	2	1	0
BORDER_COLOUR_TABLE_ADDRESS (_) ...							

Base address for the border colour table

Name	Type	MSB	LSB	Default
BORDER_COLOUR_TABLE_ADDRESS	_	37	0	0

BORDER_COLOUR_TABLE_ADDRESS

Size 38

Base address DWORD aligned for the location in memory of the border colour table for the PDM

ROGUE_CR_TPU_BORDER_COLOUR_TABLE_VDM

Size 38

Address: 0x000017a0

Access: read-write

Member of groups: tpu tpu_mcu_l0

39	38	37	36	35	34	33	32
-	BORDER_COLOUR_TABLE_ADDRESS (_) ...						

31	30	29	28	27	26	25	24

BORDER_COLOUR_TABLE_ADDRESS (_) ...

23	22	21	20	19	18	17	16
BORDER_COLOUR_TABLE_ADDRESS (_) ...							

15	14	13	12	11	10	9	8
BORDER_COLOUR_TABLE_ADDRESS (_) ...							

7	6	5	4	3	2	1	0
BORDER_COLOUR_TABLE_ADDRESS (_) ...							

Base address for the border colour table

Name	Type	MSB	LSB	Default
BORDER_COLOUR_TABLE_ADDRESS	_	37	0	0

BORDER_COLOUR_TABLE_ADDRESS

Size 38

Base address DWORD aligned for the location in memory of the border colour table for the VDM

ROGUE_CR_TPU_CEM_CDM

Size 8

Address: 0x00001810

Access: read-write

Member of groups: usc tpu tpu_mcu_l0

7	6	5	4	3	2	1	0
TAG_CEM_64_FACE_PACKING (_)	*reserved*	TAG_CEM_4K_FACE_PACKING (_)	*reserved*	TAG_CEM_FACE_PACKING (_)	TAG_CEMEDGE_DONTFILTER (_)	TAG_CEMGRAD_DONTNEGATE (_)	*reserved*

Global control to CEM textures for compute data master

Name	Type	MSB	LSB	Default
TAG_CEM_64_FACE_PACKING	_	7	7	0
TAG_CEM_4K_FACE_PACKING	_	5	5	0
TAG_CEM_FACE_PACKING	_	3	3	0
TAG_CEMEDGE_DONTFILTER	_	2	2	0
TAG_CEMGRAD_DONTNEGATE	_	1	1	0

TAG_CEMGRAD_DONTNEGATE

Size 1

Compute data master. Disable negation for user supplied gradients for cem swap i.e. will only swap dudx etc not negate

TAG_CEMEDGE_DONTFILTER

Size 1

Compute data master. Disable filtering over edges/corners for CEM. When set to 1, HW will be seemfull, ie, always stay in the current map, always honour the addressmode. When set to 0, HW will be seemless, ie, ignore addressmode, filter between faces at the edges/corners

TAG_CEM_FACE_PACKING

Size 1

Compute data master. Enable dword alignment between CEM faces when set to 1

TAG_CEM_4K_FACE_PACKING
Size 1

Compute data master. Enable 4K-byte alignment between CEM faces when set to 1. It applies for both when mipmap is enabled or disabled

TAG_CEM_64_FACE_PACKING
Size 1

Compute data master. Enable 64-byte alignment between CEM faces when set to 1. It applies for both when mipmap is enabled or disabled

---

ROGUE_CR_TPU_CEM_VDM
Size 8

Address: 0x00001800

Access: read-write

Member of groups: usc tpu tpu_mcu_l0

7	6	5	4	3	2	1	0
TAG_CEM_64_FACE_PACKING (_)	*reserved*	TAG_CEM_4K_FACE_PACKING (_)	*reserved*	TAG_CEM_FACE_PACKING (_)	TAG_CEMEDGE_DONTFILTER (_)	TAG_CEMGRAD_DONTNEGATE (_)	*reserved*

Global control to CEM textures for vertex data master

Name	Type	MSB	LSB	Default
TAG_CEM_64_FACE_PACKING	_	7	7	0
TAG_CEM_4K_FACE_PACKING	_	5	5	0
TAG_CEM_FACE_PACKING	_	3	3	0
TAG_CEMEDGE_DONTFILTER	_	2	2	0
TAG_CEMGRAD_DONTNEGATE	_	1	1	0

TAG_CEMGRAD_DONTNEGATE
Size 1

Vertex data master. Disable negation for user supplied gradients for cem swap i.e. will only swap dudx etc not negate

TAG_CEMEDGE_DONTFILTER
Size 1

Vertex data master. Disable filtering over edges/corners for CEM. When set to 1, HW will be seemfull, ie, always stay in the current map, always honour the addressmode. When set to 0, HW will be seemless, ie, ignore addressmode, filter between faces at the edges/corners

TAG_CEM_FACE_PACKING
Size 1

Vertex data master. Enable dword alignment between CEM faces when set to 1

TAG_CEM_4K_FACE_PACKING
Size 1

Vertex data master. Enable 4K-byte alignment between CEM faces when set to 1. It applies for both when mipmap is enabled or disabled

TAG_CEM_64_FACE_PACKING
Size 1

Vertex data master. Enable 64-byte alignment between CEM faces when set to 1. It applies for both when mipmap is enabled or disabled

---

ROGUE_CR_TPU_TAG_CDM_CTRL

Size 5

Address: 0x00001858

Access: read-write

Member of groups: tpu tpu_mcu_l0

7	6	5	4	3	2	1	0
-			*reserved*	AF_RATIO_TRUNCATE_TO_INTEGER (_)	AF_RATIO_TRUNCATE_TO_HALF (_)	AF_FILTERING_MODE (_)	YUV_CAM_INVALIDATE (_) ...

Global control to TAG for the compute data master

Name	Type	MSB	LSB	Default
AF_RATIO_TRUNCATE_TO_INTEGER	_	3	3	0
AF_RATIO_TRUNCATE_TO_HALF	_	2	2	0
AF_FILTERING_MODE	_	1	1	0
YUV_CAM_INVALIDATE	_	0	0	0

YUV_CAM_INVALIDATE

Size 1

When set, will invalidate YUV CSC CAM to reset the CSC coefficients. It should be set when the TPU is not performing CSC.

AF_FILTERING_MODE

Size 1

0 current mode, 1 new mode.

AF_RATIO_TRUNCATE_TO_HALF

Size 1

0 current mode, 1 truncate the fractional part of the calculated AF ratio to 0.5

AF_RATIO_TRUNCATE_TO_INTEGER

Size 1

0 current mode, 1 clear the fractional part of the calculated AF ratio

---

ROGUE_CR_USC_CLEAR_REGISTER0

Size 32

Address: 0x00004078

Access: read-write

Member of groups: pbe texas jones tornado usc

31	30	29	28	27	26	25	24
VAL (_) ...							

23	22	21	20	19	18	17	16
VAL (_) ...							

15	14	13	12	11	10	9	8
VAL (_) ...							

7	6	5	4	3	2	1	0

VAL (_) ...

Name	Type	MSB	LSB	Default
VAL	_	31	0	0

VAL
Size 32

Clear Colour register 0

ROGUE_CR_USC_CLEAR_REGISTER1
Size 32

Address: 0x00004080

Access: read-write

Member of groups: pbe texas jones tornado usc

31	30	29	28	27	26	25	24
VAL (_) ...							

23	22	21	20	19	18	17	16
VAL (_) ...							

15	14	13	12	11	10	9	8
VAL (_) ...							

7	6	5	4	3	2	1	0
VAL (_) ...							

Name	Type	MSB	LSB	Default
VAL	_	31	0	0

VAL
Size 32

Clear Colour register 1

ROGUE_CR_USC_CLEAR_REGISTER2
Size 32

Address: 0x00004088

Access: read-write

Member of groups: pbe texas jones tornado usc

31	30	29	28	27	26	25	24
VAL (_) ...							

23	22	21	20	19	18	17	16
VAL (_) ...							

15	14	13	12	11	10	9	8
VAL (_) ...							

7	6	5	4	3	2	1	0

VAL (_) ...							

Name	Type	MSB	LSB	Default
VAL	_	31	0	0

VAL
Size 32

Clear Colour register 2

ROGUE_CR_USC_CLEAR_REGISTER3
Size 32

Address: 0x00004090

Access: read-write

Member of groups: pbe texas jones tornado usc

31	30	29	28	27	26	25	24
VAL (_) ...							

23	22	21	20	19	18	17	16
VAL (_) ...							

15	14	13	12	11	10	9	8
VAL (_) ...							

7	6	5	4	3	2	1	0
VAL (_) ...							

Name	Type	MSB	LSB	Default
VAL	_	31	0	0

VAL
Size 32

Clear Colour register 3

ROGUE_CR_USC_CLEAR_REGISTER4
Size: 32

Address: 0x000042e0**Default:** 0

Type: Register**Direction**: read-write

Register banks: pbe_shared

Kick pipeline: frag_be

31	30	29	28	27	26	25	24
VAL (_) ...							

23	22	21	20	19	18	17	16
VAL (_) ...							

15	14	13	12	11	10	9	8

VAL (_) ...

7	6	5	4	3	2	1	0
VAL (_) ...							

Name	MSB	LSB	Default	Description	Bank Filter
VAL	31	0	0	Clear Colour register 4	

ROGUE_CR_USC_CLEAR_REGISTER4.VAL

Size: 32

Type: Define

Clear Colour register 4

ROGUE_CR_USC_CLEAR_REGISTER5

Size: 32

Address: 0x000042e8**Default:** 0

Type: Register**Direction**: read-write

Register banks: pbe_shared

Kick pipeline: frag_be

31	30	29	28	27	26	25	24
VAL (_) ...							

23	22	21	20	19	18	17	16
VAL (_) ...							

15	14	13	12	11	10	9	8
VAL (_) ...							

7	6	5	4	3	2	1	0
VAL (_) ...							

Name	MSB	LSB	Default	Description	Bank Filter
VAL	31	0	0	Clear Colour register 5	

ROGUE_CR_USC_CLEAR_REGISTER5.VAL

Size: 32

Type: Define

Clear Colour register 5

ROGUE_CR_USC_CLEAR_REGISTER6

Size: 32

Address: 0x000042f0**Default:** 0

Type: Register**Direction**: read-write

Register banks: pbe_shared

Kick pipeline: frag_be

31	30	29	28	27	26	25	24

VAL (_) ...

23	22	21	20	19	18	17	16
VAL (_) ...							

15	14	13	12	11	10	9	8
VAL (_) ...							

7	6	5	4	3	2	1	0
VAL (_) ...							

Name	MSB	LSB	Default	Description	Bank Filter
VAL	31	0	0	Clear Colour register 6	

ROGUE_CR_USC_CLEAR_REGISTER6.VAL

Size: 32

Type: Define

Clear Colour register 6

ROGUE_CR_USC_CLEAR_REGISTER7

Size: 32

Address: 0x000042f8**Default:** 0

Type: Register**Direction**: read-write

Register banks: pbe_shared

Kick pipeline: frag_be

31	30	29	28	27	26	25	24
VAL (_) ...							

23	22	21	20	19	18	17	16
VAL (_) ...							

15	14	13	12	11	10	9	8
VAL (_) ...							

7	6	5	4	3	2	1	0
VAL (_) ...							

Name	MSB	LSB	Default	Description	Bank Filter
VAL	31	0	0	Clear Colour register 7	

ROGUE_CR_USC_CLEAR_REGISTER7.VAL

Size: 32

Type: Define

Clear Colour register 7

ROGUE_CR_USC_G0

Size 8

Address: 0x00004098

Access: read-write

Member of groups: jones tornado bifpmcache

7	6	5	4	3	2	1	0
P (_) ...							

Name	Type	MSB	LSB	Default
P	_	7	0	0

P
Size 8

Global, cross-thread-accessible read/write register for USC programs via the 'special' bank type

ROGUE_CR_USC_G1
Size 8

Address: 0x000040a0

Access: read-write

Member of groups: jones tornado bifpmcache

7	6	5	4	3	2	1	0
P (_) ...							

Name	Type	MSB	LSB	Default
P	_	7	0	0

P
Size 8

Global, cross-thread-accessible read/write register for USC programs via the 'special' bank type

ID
Size 32

stream out primitive id field

ROGUE_CR_USC_PIXEL_OUTPUT_CTRL
Size 21

Address: 0x00004070

Access: read-write

Member of groups: texas3 texas tpu_mcu_l0 bifpmcache usc

23	22	21	20	19	18	17	16
-			PARTITION_MASK (_) ...				

15	14	13	12	11	10	9	8
PARTITION_MASK (_) ...							

7	6	5	4	3	2	1	0
PARTITION_MASK (_)					ENABLE_4TH_PARTITION (_)	WIDTH (PIXEL_WIDTH) ...	

Name	Type	MSB	LSB	Default
PARTITION_MASK	_	20	3	0x3ffff
ENABLE_4TH_PARTITION	_	2	2	0
WIDTH	PIXEL_WIDTH	1	0	0

PIXEL_WIDTH
Size 2

Possible Values:

Name	Value/Range	Info
2REGISTERS	0 [0]	
4REGISTERS	1 [0x1]	
8REGISTERS	2 [0x2]	
1REGISTER	3 [0x3]	

ENABLE_4TH_PARTITION
Size 1

Enables 4th Partition

PARTITION_MASK
Size 18

Partition Enable Mask for USC pixel task

ROGUE_CR_VBS_SO_PRIM0
Size 32

Address: 0x0000f000

Access: read-write

Member of groups: jones tiling

31	30	29	28	27	26	25	24
ID (_) ...							

23	22	21	20	19	18	17	16
ID (_) ...							

15	14	13	12	11	10	9	8
ID (_) ...							

7	6	5	4	3	2	1	0
ID (_) ...							

VBS Stream out primitive id

Name	MSB	LSB	Default
ID	31	0	---

ID
Size 32

stream out primitive id field

ROGUE_CR_VBS_SO_PRIM1

Size 32

Address: 0x0000f008

Access: read-write

Member of groups: jones tiling

31	30	29	28	27	26	25	24
ID (_) ...							

23	22	21	20	19	18	17	16
ID (_) ...							

15	14	13	12	11	10	9	8
ID (_) ...							

7	6	5	4	3	2	1	0
ID (_) ...							

VBS Stream out primitive id

Name	MSB	LSB	Default
ID	31	0	---

ID

Size 32

stream out primitive id field

ROGUE_CR_VBS_SO_PRIM2

Size 32

Address: 0x0000f010

Access: read-write

Member of groups: jones tiling

31	30	29	28	27	26	25	24
ID (_) ...							

23	22	21	20	19	18	17	16
ID (_) ...							

15	14	13	12	11	10	9	8
ID (_) ...							

7	6	5	4	3	2	1	0
ID (_) ...							

VBS Stream out primitive id

Name	MSB	LSB	Default
ID	31	0	---

ROGUE_CR_VBS_SO_PRIM3

Size 32

Address: 0x0000f018

Access: read-write

Member of groups: jones tiling

31	30	29	28	27	26	25	24
ID (_) ...							

23	22	21	20	19	18	17	16
ID (_) ...							

15	14	13	12	11	10	9	8
ID (_) ...							

7	6	5	4	3	2	1	0
ID (_) ...							

VBS Stream out primitive id

Name	MSB	LSB	Default
ID	31	0	---

ID

Size 32

stream out primitive id field

ROGUE_CR_VDM_BATCH

Size 14

Address: 0x00000420

Access: read-write

Member of groups: jones tornado hub

15	14	13	12	11	10	9	8
-	NUMBER (_) ...						

7	6	5	4	3	2	1	0
NUMBER (_) ...							

The Batch number is a index list block (draw call) ID which is passed through the GPU pipeline. This is helpful for debug and performance profiling. The starting batch number should be programmed before the first TA phase of every frame The VDM will increment it on every Index List Block across TA phases until reset This register needs to be saved/restored for each context

Name	Type	MSB	LSB	Default
NUMBER	_	13	0	---

NUMBER

Size 14

ROGUE_CR_VDM_CALL_STACK_POINTER

Size 40

Address: 0x00000418

Access: read-write

Member of groups: jones tornado hub

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)					*reserved*		

The pointer to the control stream call stack. The current pointer within the VDM's call stack in external memory. The call stack is used whenever a call is made to another control stream, to store the return address (location in current control stream). This register should be programmed before each TA which uses a call stack This register needs to be saved/restored for each context

Name	Type	MSB	LSB	Default
ADDR	_	39	3	---

ADDR

Size 37

1TB range, 64-bit aligned base address

ROGUE_CR_VDM_CONTEXT_RESUME_TASK0

Size 64

Address: 0x00000450

Access: read-write

Member of groups: jones tornado hub

63	62	61	60	59	58	57	56
PDS_STATE1 (_) ...							

55	54	53	52	51	50	49	48
PDS_STATE1 (_) ...							

47	46	45	44	43	42	41	40
PDS_STATE1 (_) ...							

39	38	37	36	35	34	33	32
PDS_STATE1 (_)							

31	30	29	28	27	26	25	24
PDS_STATE0 (_) ...							

23	22	21	20	19	18	17	16
PDS_STATE0 (_) ...							

15	14	13	12	11	10	9	8

PDS_STATE0 (_) ...							

7	6	5	4	3	2	1	0
PDS_STATE0 (_) ...							

These words define the PDS State Update task which will be written by the VDM to its context resume control stream on a context store operation. The function of this task is described in the Rogue Context Switching Hardware Specifiction. Their format is defined in the TRM. This register must be programmed before writing to VDM_CONTEXT_STORE_START_PULSE.

Name	Type	MSB	LSB	Default
PDS_STATE1	_	63	32	---
PDS_STATE0	_	31	0	---

PDS_STATE1
Size 32

PDS_STATE0
Size 32

ROGUE_CR_VDM_CONTEXT_RESUME_TASK1
Size 32

Address: 0x00000458

Access: read-write

Member of groups: jones tornado hub

31	30	29	28	27	26	25	24
PDS_STATE2 (_) ...							

23	22	21	20	19	18	17	16
PDS_STATE2 (_) ...							

15	14	13	12	11	10	9	8
PDS_STATE2 (_) ...							

7	6	5	4	3	2	1	0
PDS_STATE2 (_) ...							

This word defines the PDS State Update task which will be written by the VDM to its context resume control stream on a context store operation. The function of this task is described in the Rogue Context Switching Hardware Specifiction. Its format is defined in the TRM. This register must be programmed before writing to VDM_CONTEXT_STORE_START_PULSE.

Name	Type	MSB	LSB	Default
PDS_STATE2	_	31	0	---

PDS_STATE2
Size 32

ROGUE_CR_VDM_CONTEXT_RESUME_TASK2
Size 64

Address: 0x00000460

Access: read-write

Member of groups: jones tornado hub

63	62	61	60	59	58	57	56
STREAM_OUT2 (_) ...							

55	54	53	52	51	50	49	48
STREAM_OUT2 (_) ...							

47	46	45	44	43	42	41	40
STREAM_OUT2 (_) ...							

39	38	37	36	35	34	33	32
STREAM_OUT2 (_)							

31	30	29	28	27	26	25	24
STREAM_OUT1 (_) ...							

23	22	21	20	19	18	17	16
STREAM_OUT1 (_) ...							

15	14	13	12	11	10	9	8
STREAM_OUT1 (_) ...							

7	6	5	4	3	2	1	0
STREAM_OUT1 (_) ...							

These words defines the Stream Out Sync program which will be written, as a PPP State Update, by the VDM to its context resume control stream on a context store operation The function of this task is described in the Rogue Context Switching Hardware Specifiction Its format is defined in the TRM. This register must be programmed before writing to VDM_CONTEXT_STORE_START_PULSE.

Name	Type	MSB	LSB	Default
STREAM_OUT2	_	63	32	---
STREAM_OUT1	_	31	0	---

STREAM_OUT2

Size 32

STREAM_OUT1

Size 32

ROGUE_CR_VDM_CONTEXT_RESUME_TASK3

Size 64

Address: 0x0000f068

Access: read-write

Member of groups: jones

63	62	61	60	59	58	57	56
PDS_STATE1 (_) ...							

55	54	53	52	51	50	49	48
PDS_STATE1 (_) ...							

47	46	45	44	43	42	41	40
PDS_STATE1 (_) ...							

39	38	37	36	35	34	33	32
PDS_STATE1 (_)							

31	30	29	28	27	26	25	24
PDS_STATE0 (_) ...							

23	22	21	20	19	18	17	16
PDS_STATE0 (_) ...							

15	14	13	12	11	10	9	8
PDS_STATE0 (_) ...							

7	6	5	4	3	2	1	0
PDS_STATE0 (_) ...							

These words define the PDS State Update task which will be written by the VDM to its context resume control stream on a context store operation. The function of this task is described in the Rogue Context Switching Hardware Specifiction. Their format is defined in the TRM. This register must be programmed before writing to VDM_CONTEXT_STORE_START_PULSE.

Name	MSB	LSB	Default
PDS_STATE1	63	32	---
PDS_STATE0	31	0	---

PDS_STATE1

Size 32

PDS_STATE0

Size 32

ROGUE_CR_VDM_CONTEXT_RESUME_TASK4

Size 32

Address: 0x0000f070

Access: read-write

Member of groups: jones

31	30	29	28	27	26	25	24
PDS_STATE2 (_) ...							

23	22	21	20	19	18	17	16
PDS_STATE2 (_) ...							

15	14	13	12	11	10	9	8
PDS_STATE2 (_) ...							

7	6	5	4	3	2	1	0
PDS_STATE2 (_) ...							

This word defines the PDS State Update task which will be written by the VDM to its context resume control stream on a context store operation. The function of this task is described in the Rogue Context Switching Hardware Specifiction. Its format is defined in the TRM. This register must be programmed before writing to VDM_CONTEXT_STORE_START_PULSE.

Name	MSB	LSB	Default
PDS_STATE2	31	0	---

PDS_STATE2
Size 32

<

PDS_STATE1
Size 32

PDS_STATE0
Size 32

ROGUE_CR_VDM_CONTEXT_RESUME_TASK4
Size 32

Address: 0x0000f070

Access: read-write

Member of groups: jones

31	30	29	28	27	26	25	24
PDS_STATE2 (_) ...							

23	22	21	20	19	18	17	16
PDS_STATE2 (_) ...							

15	14	13	12	11	10	9	8
PDS_STATE2 (_) ...							

7	6	5	4	3	2	1	0
PDS_STATE2 (_) ...							

This word defines the PDS State Update task which will be written by the VDM to its context resume control stream on a context store operation. The function of this task is described in the Rogue Context Switching Hardware Specifiction. Its format is defined in the TRM. This register must be programmed before writing to VDM_CONTEXT_STORE_START_PULSE.

Name	MSB	LSB	Default
PDS_STATE2	31	0	---

PDS_STATE2
Size 32

ROGUE_CR_VDM_CONTEXT_STATE_BASE
Size 40

Address: 0x00000428

Access: read-write

Member of groups: blackpearl jones tornado hub

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16

ADDR (_) ...

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)				*reserved*			

The base address in external memory of the VDM's context state buffer. On a context store the VDM will store its state to this address, and reload it on a context resume. The size and format of the data written is defined in the LLS section of the TRM. This register must be programmed before initiating a context store by writing to VDM_CONTEXT_STORE_START_PULSE.

Name	Type	MSB	LSB	Default
ADDR	_	39	4	---

ADDR

Size 36

1TB range, 128-bit aligned base address

ROGUE_CR_VDM_CONTEXT_STORE_TASK0

Size 64

Address: 0x00000438

Access: read-write

Member of groups: jones tornado hub

63	62	61	60	59	58	57	56
PDS_STATE1 (_) ...							

55	54	53	52	51	50	49	48
PDS_STATE1 (_) ...							

47	46	45	44	43	42	41	40
PDS_STATE1 (_) ...							

39	38	37	36	35	34	33	32
PDS_STATE1 (_)							

31	30	29	28	27	26	25	24
PDS_STATE0 (_) ...							

23	22	21	20	19	18	17	16
PDS_STATE0 (_) ...							

15	14	13	12	11	10	9	8
PDS_STATE0 (_) ...							

7	6	5	4	3	2	1	0
PDS_STATE0 (_) ...							

These words define the PDS State Update task which will be inserted into the VDM pipeline on a context store operation. The function of this task is described in the Rogue Context Switching Hardware Specification. Their format is defined in the TRM. This register must be programmed before writing to VDM_CONTEXT_STORE_START_PULSE.

Name	Type	MSB	LSB	Default
PDS_STATE1	_	63	32	---

PDS_STATE0	_	31	0	---

PDS_STATE1
Size 32

PDS_STATE0
Size 32

ROGUE_CR_VDM_CONTEXT_STORE_TASK1
Size 32

Address: 0x00000440

Access: read-write

Member of groups: jones tornado hub

31	30	29	28	27	26	25	24
PDS_STATE2 (_) ...							

23	22	21	20	19	18	17	16
PDS_STATE2 (_) ...							

15	14	13	12	11	10	9	8
PDS_STATE2 (_) ...							

7	6	5	4	3	2	1	0
PDS_STATE2 (_) ...							

This word defines the PDS State Update task which will be inserted into the VDM pipeline on a context store operation. The function of this task is described in the Rogue Context Switching Hardware Specification. Its format is defined in the TRM. This register must be programmed before writing to VDM_CONTEXT_STORE_START_PULSE.

Name	Type	MSB	LSB	Default
PDS_STATE2	_	31	0	---

PDS_STATE2
Size 32

ROGUE_CR_VDM_CONTEXT_STORE_TASK2
Size 64

Address: 0x00000448

Access: read-write

Member of groups: jones tornado hub

63	62	61	60	59	58	57	56
STREAM_OUT2 (_) ...							

55	54	53	52	51	50	49	48
STREAM_OUT2 (_) ...							

47	46	45	44	43	42	41	40
STREAM_OUT2 (_) ...							

39	38	37	36	35	34	33	32

STREAM_OUT2 (_)							

31	30	29	28	27	26	25	24
STREAM_OUT1 (_) ...							

23	22	21	20	19	18	17	16
STREAM_OUT1 (_) ...							

15	14	13	12	11	10	9	8
STREAM_OUT1 (_) ...							

7	6	5	4	3	2	1	0
STREAM_OUT1 (_) ...							

These words defines the Stream Out Sync program which will be inserted into the VDM pipeline as a PPP State Update on a context store operation. The function of this task is described in the Rogue Context Switching Hardware Specification. Its format is defined in the TRM. This register must be programmed before writing to VDM_CONTEXT_STORE_START_PULSE.

Name	Type	MSB	LSB	Default
STREAM_OUT2	_	63	32	---
STREAM_OUT1	_	31	0	---

STREAM_OUT2

Size 32

STREAM_OUT1

Size 32

ROGUE_CR_VDM_CONTEXT_STORE_TASK3

Size 64

Address: 0x0000f058

Access: read-write

Member of groups: jones

63	62	61	60	59	58	57	56
PDS_STATE1 (_) ...							

55	54	53	52	51	50	49	48
PDS_STATE1 (_) ...							

47	46	45	44	43	42	41	40
PDS_STATE1 (_) ...							

39	38	37	36	35	34	33	32
PDS_STATE1 (_)							

31	30	29	28	27	26	25	24
PDS_STATE0 (_) ...							

23	22	21	20	19	18	17	16
PDS_STATE0 (_) ...							

15	14	13	12	11	10	9	8

PDS_STATE0 (_) ...

7	6	5	4	3	2	1	0
PDS_STATE0 (_) ...							

These words define the PDS State Update task which will be inserted into the VDM pipeline on a context store operation. The function of this task is described in the Rogue Context Switching Hardware Specification. Their format is defined in the TRM. This register must be programmed before writing to VDM_CONTEXT_STORE_START_PULSE.

Name	MSB	LSB	Default
PDS_STATE1	63	32	---
PDS_STATE0	31	0	---

PDS_STATE1

Size 32

PDS_STATE0

Size 32

ROGUE_CR_VDM_CONTEXT_STORE_TASK4

Size 32

Address: 0x0000f060

Access: read-write

Member of groups: jones

31	30	29	28	27	26	25	24
PDS_STATE2 (_) ...							

23	22	21	20	19	18	17	16
PDS_STATE2 (_) ...							

15	14	13	12	11	10	9	8
PDS_STATE2 (_) ...							

7	6	5	4	3	2	1	0
PDS_STATE2 (_) ...							

This word defines the PDS State Update task which will be inserted into the VDM pipeline on a context store operation. The function of this task is described in the Rogue Context Switching Hardware Specification. Its format is defined in the TRM. This register must be programmed before writing to VDM_CONTEXT_STORE_START_PULSE.

Name	MSB	LSB	Default
PDS_STATE2	31	0	---

PDS_STATE2

Size 32

63	62	61	60	59	58	57	56
PDS_STATE1 (_) ...							

55	54	53	52	51	50	49	48
PDS_STATE1 (_) ...							

47	46	45	44	43	42	41	40

PDS_STATE1 (_) ...

39	38	37	36	35	34	33	32
PDS_STATE1 (_)							

31	30	29	28	27	26	25	24
PDS_STATE0 (_) ...							

23	22	21	20	19	18	17	16
PDS_STATE0 (_) ...							

15	14	13	12	11	10	9	8
PDS_STATE0 (_) ...							

7	6	5	4	3	2	1	0
PDS_STATE0 (_) ...							

These words define the PDS State Update task which will be written by the VDM to its context resume control stream on a context store operation. The function of this task is described in the Rogue Context Switching Hardware Specifiction. Their format is defined in the TRM. This register must be programmed before writing to VDM_CONTEXT_STORE_START_PULSE.

Name	MSB	LSB	Default
PDS_STATE1	63	32	---
PDS_STATE0	31	0	---

ROGUE_CR_VDM_CTRL_STREAM_BASE

Size 40

Address: 0x00000408

Access: read-write

Member of groups: jones tornado hub

39	38	37	36	35	34	33	32
ADDR (_) ...							

31	30	29	28	27	26	25	24
ADDR (_) ...							

23	22	21	20	19	18	17	16
ADDR (_) ...							

15	14	13	12	11	10	9	8
ADDR (_) ...							

7	6	5	4	3	2	1	0
ADDR (_)						*reserved*	

The base address of the Vertex Data Master's Input Parameter Control Stream in external memory

Name	Type	MSB	LSB	Default
ADDR	_	39	2	---

ADDR

Size 38

1TB range, 32-bit aligned base address

ROGUE_CR_VDM_DRAW_INDIRECT0

Size 64

Address: 0x0000f038

Access: read-write

Member of groups: blackpearl

63	62	61	60	59	58	57	56
PDS_STATE1 (_) ...							

55	54	53	52	51	50	49	48
PDS_STATE1 (_) ...							

47	46	45	44	43	42	41	40
PDS_STATE1 (_) ...							

39	38	37	36	35	34	33	32
PDS_STATE1 (_)							

31	30	29	28	27	26	25	24
PDS_STATE0 (_) ...							

23	22	21	20	19	18	17	16
PDS_STATE0 (_) ...							

15	14	13	12	11	10	9	8
PDS_STATE0 (_) ...							

7	6	5	4	3	2	1	0
PDS_STATE0 (_) ...							

These words define the PDS State Update task which will run before any DrawIndirect calls. Their format is defined in the TRM. This register must be programmed before writing to VDM_START_PULSE.

Name	MSB	LSB	Default
PDS_STATE1	63	32	---
PDS_STATE0	31	0	---

PDS_STATE1

Size 32

PDS_STATE0

Size 32

ROGUE_CR_VDM_DRAW_INDIRECT1

Size 32

Address: 0x0000f040

Access: read-write

Member of groups: blackpearl

31	30	29	28	27	26	25	24
PDS_STATE2 (_) ...							

23	22	21	20	19	18	17	16
PDS_STATE2 (_) ...							

15	14	13	12	11	10	9	8
PDS_STATE2 (_) ...							

7	6	5	4	3	2	1	0
PDS_STATE2 (_) ...							

This word define the PDS State Update task which will run before any DrawIndirect calls. Its format is defined in the TRM. This register must be programmed before writing to VDM_START_PULSE.

Name	MSB	LSB	Default
PDS_STATE2	31	0	---

PDS_STATE2

Size 32